OPTIMIZATION OF PHOSPHORUS EMITTER USING $POCl_3$ DIFFUSION FOR PERC CELLS

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ABSTRACT

OPTIMIZATION OF PHOSPHORUS EMITTER USING POCl3 DIFFUSION FOR PERC CELLS

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The active dopant profile and the enhanced passivation of the emitter are keys to improving passivated emitter and rear contact (PERC) solar cell efficiency. PERC cells evolved from the standard Al-BSF cells that suffered from recombination losses due to full-area metal contact at the rear side. PERC cell technology enables to reduce the metal contact fraction and considering the total saturation current density (J_0), the emitter region has the biggest share. In this work, the optimization of the profile and the passivation of the emitter are investigated. Emitters are formed by using a liquid source phosphoryl chloride ($POCl_3$) diffusion process. By varying drive-in conditions, desired profiles can be formed for phosphorus diffused regions. Enhancement in the passivation is observed on the symmetrical emitter samples by using thermally grown silicon dioxide due to its low interface defect density (D_{it}). In addition, we show that a low temperature annealing process (LTA) at 700°C for 60 minutes after the silicon nitride (SiN_x) deposition improves the surface and the bulk passivation especially for emitters with high surface concentrations (≈3E20 cm^{-3}). According to the results of the symmetrical emitter samples, the saturation current

density of the emitter ($J_{0,e}$) is reduced from 100 to 60 fA/cm^2 by varying the profile without changing the sheet resistance and below 40 fA/cm^2 by increasing the sheet resistance.

Keywords: liquid source diffusion, emitter, passivation

ÖZ

PERC TİPİ HÜCRELER İÇİN POCl3 DİFÜZYONU İLE EMİTÖR OPTİMİZASYONU

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Aktif katkı profili ve geliştirilmiş pasivasyon, PERC tipi güneş hücresi verimliliğini iyileştirmenin anahtarıdır. PERC hücreleri, arka taraftaki tam alan metal kontağı nedeniyle rekombinasyon kayıplarından muzdarip olan standart Al-BSF güneş hücrelerinden geliştirilmiştir. PERC hücre teknolojisi, arka taraf metal kontak oranının azaltılmasına olanak sağlar. Toplam doygunluk akım yoğunluğu (J_0) dikkate alındığında emitör bölgesi en büyük paya sahiptir. Bu çalışmada, profilin optimizasyonu ve emitörün pasivasyonu incelenmiştir. Emitörler, sıvı kaynaklı bir fosforil klorür ($POCl_3$) difüzyon işlemi kullanılarak oluşturulmuştur. Sürme koşulları değiştirilerek, fosfor difüzyonlu bölgeler için istenilen profiller oluşturulabilir. Düşük arayüz kusur yoğunluğuna sahip olması nedeniyle termal olarak büyütülmüş silikon dioksitin emitör pasivasyonunu iyileştirdiği simetrik emitör örneklerinde gözlemlenmiştir. Ek olarak, silisyum nitrür (SiN_x) biriktirme işleminden sonra 700°C'de 1 saat boyunca uygulanan bir tavlama işleminin yüzey ve gövde pasivasyonunu iyileştirdiğini gösteriyoruz. Simetrik emitör örneklerinin sonuçlarına göre, emitör levha direnci değiştirilmeden, profil değiştirilerek emitörün

doyma akım yoğunluğu ($J_{0,e}$) 100'den 60 fA/cm^2'ye, levha direnci arttırılarak da 40 fA/cm^2'nin altına düşürülmüştür.

Anahtar Kelimeler: sıvı kaynak difüzyon, emitör, pasivasyon

To *my family*

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CHAPTER 1

INTRODUCTION

Fossil fuels are carbon-rich materials that can produce electricity by burning. During production, a large amount of CO_2 is emitted. Fossil fuel-fired power plants cause 33%-40% of global CO_2 emissions [1], [2]. CO_2 absorbs sunlight and leads the planet to get hotter. Due to the increase in CO_2 in the atmosphere in the last decades, global warming has become one of the greatest threats to the World. To reduce carbon emissions, renewable energy sources are safe, reliable and low-or-zero carbon footprint alternatives to generate useful energy. Enhancement in the wind, geothermal, biomass, hydro, tidal and solar energy satisfies the important part of this demand. Along with wind energy, solar energy is one of the most popular renewable energy sources. Energy can be generated from sunlight via different applications. Recently, photovoltaics (PV) applications have become favorable due to cost reduction, increased power conversion efficiency (PCE) and longer lifetime of modules. Also, researches show that carbon emission from PV systems is 10 to 53 orders of magnitude lower than oil-fired steam-generating energy systems [3], [4]. In PV, direct current (DC) electricity is generated by a solar cell which is any device that directly converts light energy into electrical energy through the photovoltaic effect. Then, the DC electricity generated by solar cells is converted into alternative current (AC) electricity which the electrical grid uses. The schematic of this conversion is shown in Figure 1.1.

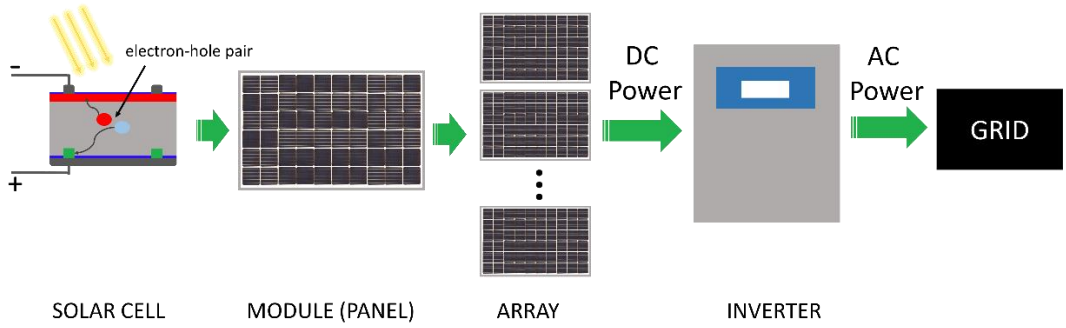

Figure 1.1. The configuration of the PV system from solar cell to grid

1.1 Silicon Solar Cells

Silicon (Si) based solar cells are the dominant technology in the PV industry because solar cells made from Si provide high efficiency, long lifetime and low cost at the same time. Due to the simplicity and the low cost of production, c-Si homojunction solar cells dominate the PV market. Homojunction is an interface between two similar semiconductor materials with the same band gaps but doped with different materials. In PV, p-type Si wafers doped with boron (B) or n-type Si wafers doped with phosphorus (P) are generally used as bulk materials. Then, to form a homojunction, which is also called as p-n junction, p-type and n-type semiconductor materials are merged. The way to form p-n junction on the p-type or n-type Si wafers is by doping the material with opposite polarity. The capability of processing more than 1000 wafers simultaneously in a single process with high quality makes the liquid source diffusion favorable in industry and research. For passivated emitter and rear contact (PERC) solar cells, p-type Si wafers are used and phosphorus oxychloride ($POCl_3$) diffusion is realized to form an n+ emitter region. The amount of resistance and recombination that existed in the device limits the efficiency of a solar cell. Since the standard Al-BSF solar cells are replaced with PERC solar cells; metallized regions, which act as recombination centers, in the solar cells are reduced significantly. Thus, the emitter region has the biggest contribution to the total amount of recombination in the PERC solar cells

1.1.1 Recombination in Emitter

The excess number of dopants in specific regions is one of the major recombination losses. PERC cells have reduced back surface field (BSF) regions compared to standard Al-BSF solar cells. However, the emitter region is similar for both cell types. Considering the total saturation current density, the emitter has the highest contribution in PERC solar cells. Although the metallized areas are more recombinative than passivated emitter regions, the metal fraction is very low compared to passivated areas. Regions in emitter with doping concentrations higher than 1E20 cm^{-3} are called as dead layer. Due to high doping concentration in the dead layer, the Auger recombination mechanism becomes dominant and leads to losses in open circuit voltage (V_{oc}) and short circuit current (J_{sc}). Therefore, an enhancement in the PCE is possible simply by increasing the sheet resistance, i.e., decreasing the amount of dopant, which will reduce the recombination. However, contact resistivity and recombination between the emitter and the metal contacts will increase due to reduced dopants. Developments in the metal pastes enable to get good contact from these emitters with high sheet resistance. Moreover, the selective emitter approach, which is additional doping only under the metal contacts, allows emitters with fewer dopants. Another way to reduce the recombination in the emitter is the enhancement of the passivation layer. By depositing or growing an optimized stack of layers on the emitter, dangling bonds on the surface can be saturated and optimum amount of hydrogen (H) to passivate the bulk and the surface can be provided.

1.1.2 Solar Cell Parameters

Parameters like V_{oc}, I_{sc} and fill factor (FF) are used to characterize the performance of a solar cell. All these parameters are determined with an IV measurement under standard test conditions (STC). These conditions dictate that solar cells should be measured at 25°C, under 1-sun illumination with a total irradiance of 1000 W/m^2 and the AM1.5 spectrum should be used.

V_{oc} of a solar cell is the maximum voltage available from a solar cell which occurs when no current flows through the external circuit. Voc of a solar cell depends on the light-generated current (I_L) and dark saturation current (I_0) and the equation when the net current is equal to zero is:

$$V_{oc} = \frac{nkT}{q} ln\left(\frac{I_L}{I_0} + 1\right) \quad \text{Eq.1}$$

One can expect that increasing temperature also increases the V_{oc}. However, I_0 depends on the temperature and due to changes in intrinsic carrier concentration (n_i), I_0 increases rapidly.

I_{sc} is the current flows through the external circuit when the electrodes are short-circuited, which means the voltage across the solar cell is zero. I_{sc} is the maximum current that may be drawn from the solar cell. I_{sc} depends on the area of the solar cell, the number of photons, the optical properties of the cell (absorption, reflection and transmission) and the spectrum.

FF is the ratio of maximum power that can be obtained from a solar cell and the product of V_{oc} and J_{sc}. For open-circuit and short-circuit conditions, the net power of the solar cell is zero. IV curve of the solar cell is affected by the resistive effects (shunt and series resistance). Series resistance does not affect the V_{oc} of the solar cell, but series resistance has an impact on the IV curve near the V_{oc}. On the other hand, shunt resistance strongly affects the IV curve near the I_{sc}. Figure 1.2 shows an ideal IV curve and IV curve with the effect of series and shunt resistances.

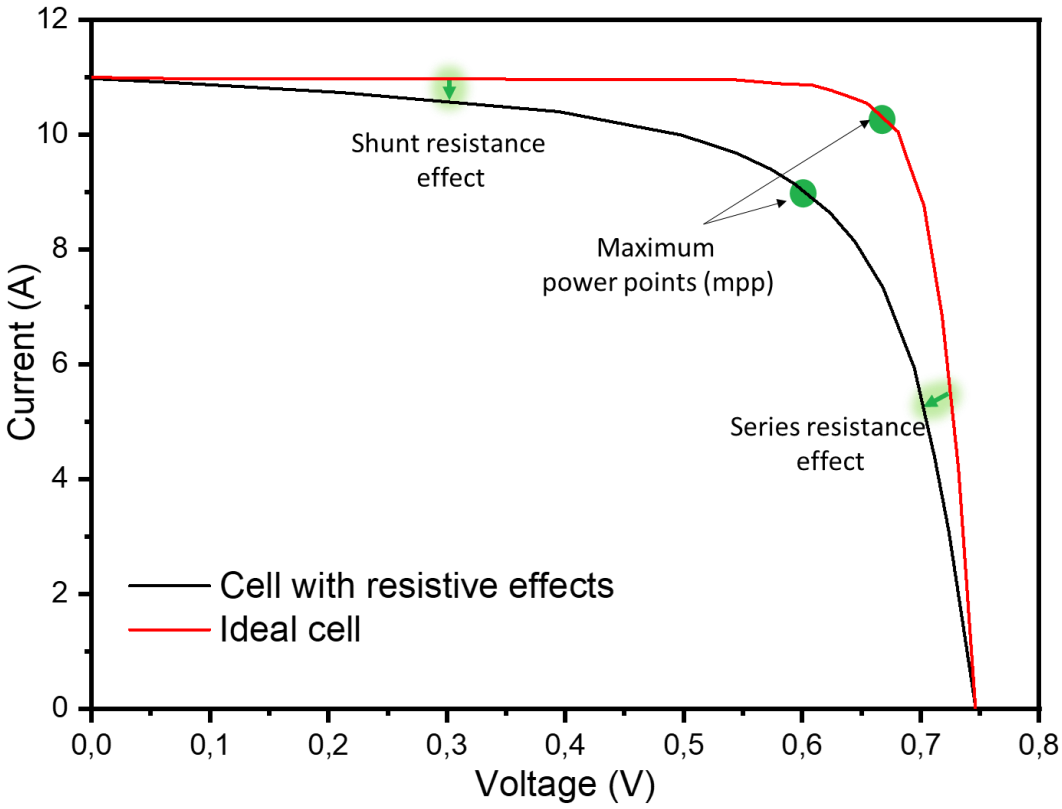

Figure 1.2. IV graph of an ideal cell and the cell with series and shunt resistance

CHAPTER 2

LITERATURE REVIEW

2.1 Fundamentals of Diffusion Process

Diffusion process is commonly used to make Si crystal p-type and n-type, respectively. Using a continuum approach, diffusion process can be well described by Fick's laws. Eq.2 is Fick's first law of diffusion,

$$J = -D\frac{\partial C(x,t)}{\partial x} \quad \text{Eq.2}$$

Where *C* is the impurity concentration, *D* is the diffusion coefficient, and *J* is the net flux of material. The negative sign on the right-hand side of the equation means that the diffusion direction is through decreasing concentration.

Due to the difficulty in detecting the diffusing material, measuring the current density of the impurity is not convenient. Another expression has been developed for that purpose. In Eq.3, measurable quantities are used by assuming a long bar material with a uniform cross-section A, a small volume of length dx. The flux of material entering and leaving the material is shown as J_2 and J_1, respectively.

$$\frac{J_2 - J_1}{dx} = \frac{\partial J}{\partial x} \quad \text{Eq.3}$$

In the case of unequal J_2 and J_1, the dopant concentration in the volume must change. In a unit volume, the number of dopants is the product of the concentration and the differential volume element. Thus:

$$\frac{dN}{dt} = Adx\frac{\partial C}{\partial t} = -A(J_2 - J_1) = -Adx\frac{\partial J}{\partial x}$$

Where N is the number of impurities in the volume element, or

$$\frac{\partial C(x,t)}{\partial t} = -\frac{\partial J}{\partial x} \quad \text{Eq.4}$$

By using Fick's first law, Eq.4 can be expressed as:

$$\frac{\partial C(x,t)}{\partial t} = \frac{\partial}{\partial x}\left(D\frac{\partial C}{\partial x}\right) \quad \text{Eq.5}$$

The most common expression of Fick's second law is Eq.5. The interested direction is the z, which is into the wafer and if it is assumed that the diffusion coefficient is independent of position:

$$\frac{\partial C(z,t)}{\partial t} = D\frac{\partial^2 C(z,t)}{\partial z^2} \quad \text{Eq.6}$$

Finally, in three dimensions for an isotropic medium, Fick's second law is expressed as:

$$\frac{\partial C}{\partial t} = D\nabla^2 C \quad \text{Eq.7}$$

2.2 $POCl_3$ Diffusion Mechanism

For P doping, the chemical $POCl_3$ is used in the liquid form. In section 3.1.3, it is explained how $POCl_3$, N_2 and O_2 are supplied into the tube furnace. In this section, a detailed explanation of the mechanism of $POCl_3$ diffusion will be given.

2.2.1 Pre-deposition

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2 \quad \text{Eq.8}$$

During the pre-deposition step, at the inlet of the tube furnace, N_2 carried $POCl_3$ and O_2 meets. At high temperatures, $POCl_3$ decomposes and the reaction defined by Eq.8 is realized [5]. Phosphorus oxide (P_2O_5) is one of the products of the reaction and

carries P atoms to the surface of the Si wafer. Chlorine (Cl_2) leaves the system without involving any reaction.

$$Si + O_2 \rightarrow SiO_2 \quad \text{Eq.9}$$

$$SiO_2 + P_2O_5 \rightarrow SiO_2.P_2O_5 \quad \text{Eq.10}$$

While the reaction in Eq.8 is continuously realized, the reaction in Eq.9 is also occurred. SiO_2 is formed at the surface of the Si wafer by the reaction of Si interstitials and O_2. After that, P_2O_5 reaches the Si wafer surface and PSG is formed as a product of the reaction in Eq.10. Composition of the PSG may vary with the process parameters, especially changes in the ratio of $POCl_3/O_2$ during the pre-deposition.

$$5Si + 2P_2O_5 \rightarrow 5SiO_2 + 4P \quad \text{Eq.11}$$

At this point, PSG is formed on the Si wafer, and a SiO_2 layer still exists between PSG and Si surface. In Figure 2.1, the current structure after the pre-deposition step is illustrated. While the $POCl_3$, O_2 and N_2 gas flows are active and chemical reactions in Eq.8, Eq.9 and Eq.10 are occurred, Si interstitials start to move from the Si wafer to the PSG layer through the SiO_2 layer. When they reach the PSG layer, the chemical reaction in Eq.11 takes place and free P atoms are released. These free P atoms move from PSG to the Si surface through the SiO_2 layer and diffuse into the wafer.

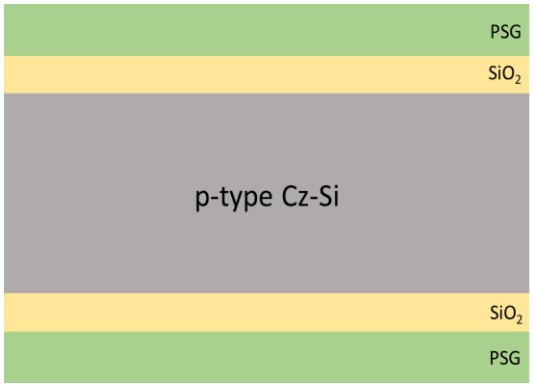

Figure 2.1. Schematic of the wafer after the pre-deposition step of the diffusion process.

2.2.2 Drive-In

After the pre-deposition step, desired PSG is formed and this layer acts as an infinite source. During the pre-deposition step, a certain amount of P atoms is diffused into the Si wafer. A drive-in process generally in higher temperatures is introduced after the pre-deposition step to send more P atoms into bulk further and obtain a deeper profile. Depending on the temperature, time and ambient conditions, the profile of the diffused regions changes. The drive-in step can be divided into two categories.

2.2.2.1 N_2 Drive-In

N_2 is an inert gas under tube furnace conditions. This implies that N_2 ambient does not cause a direct change in the PSG and Si wafer. $POCl_3$ carried by N_2 and O_2 gas flows are closed. Therefore, unlike reactions in Eq.11 and Eq.12; Eq.8, Eq.9 and Eq.10 are inactive during N_2 drive-in. In Eq.11, Si interstitials react with P_2O_5 in the PSG and form SiO_2 and free P atoms, which diffuse from PSG to the Si wafer. Also, the reaction in Eq.12 is realized and excess SiO_2 dissolves in the PSG layer.

$$SiO_2 + xSiO_2.P_2O_5 \rightarrow (x+1)SiO_2.P_2O_5 \qquad \text{Eq.12}$$

Jäger et al. have shown a temperature-dependent equilibrium SiO_2 thickness for drive-in under N_2 ambient [5]. They propose that these two reactions are in a dynamic balance when the equilibrium thickness is reached. Suppose the SiO_2 thickness is bigger than the equilibrium thickness. In that case, excess SiO_2 will be dissolved in the PSG or if the SiO_2 thickness is smaller than the equilibrium, then the reaction in Eq.11 will be dominant and growth of the SiO_2 will be observed until it reaches equilibrium thickness. These mechanisms are shown in Figure 2.2.

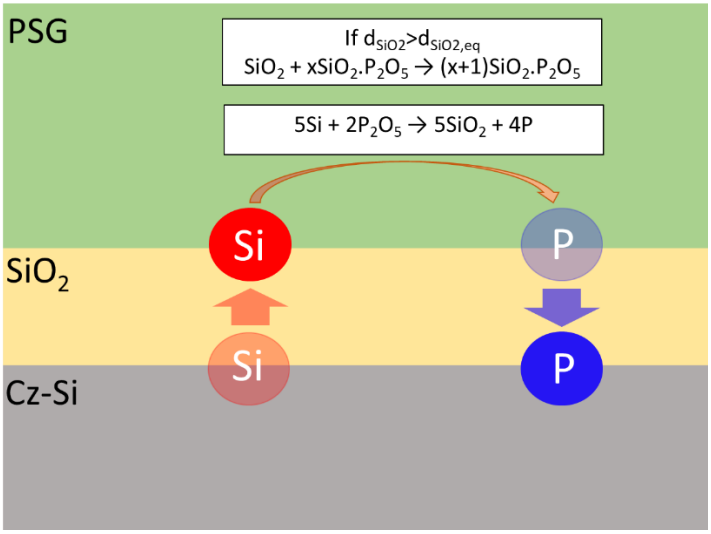

Figure 2.2. Diffusion mechanism during N_2 drive-in

Under N_2 ambient, if the SiO_2 thickness is equal to or lower than the equilibrium thickness, P will be continuously transitioned from PSG to Si wafer. Increasing the process temperature will increase P diffusivity and more P atoms will diffuse into the Si wafer [5], [6]. Also, by increasing the duration of the drive-in step, more P atoms will be allowed to diffuse even if the temperature is the same.

2.2.2.2 O_2 Drive-In

In Eq.9 and Eq.13, O_2 oxidizes the Si and P, respectively. If there is a flow of oxygen during the drive-in, it will affect P diffusion into the Si wafer or Si interstitial diffusion from the Si wafer to PSG. Several ideas have been proposed to explain how drive-in under O_2 ambient suppresses the P diffusion from PSG to Si wafer. Werner et al. have shown that a drive-in step under an ambient containing 100% O_2 increases the SiO_2 thickness [7]. For a diffusion process with 10 and 60 minutes of drive-in steps under O_2 ambient, almost the same amount of P diffuses into the Si wafer. Therefore, they claim that if the SiO_2 thickness exceeds a critical point, it will block P diffusion into the Si. On the other hand, Li et al. reported that SiO_2 thickness is independent of the process conditions and this intermediate SiO_2 thickness is around 5.5 nm [8]. Also, since the SiO_2 thickness is the same for all cases, they claim that

blockage of the P diffusion into Si is due to the reaction in Eq.13, which is the oxidation of free P atoms.

$$5O_2 + 4P \rightarrow 2P_2O_5 \qquad \text{Eq.13}$$

Finally, a comprehensive study by Jäger et al. showed that the main mechanism of restraining P diffusion during drive-in under O_2 ambient is the oxidation of Si interstitial diffuses from Si wafer to PSG [5].

Table 2.1. Recipe parameters and experimental results for recipes at 829°C for all process steps [5]

Recipe	Temperature [°C]	Drive-In O_2 [min]	Drive-In N_2 [min]	Thickness of SiO_2 [nm]	RSheet [Ω/□]	NSurface [cm^{-3}]
A1	829	0	0	2.8 ± 0.5	455 ± 138	2E19
A2	829	5	0	1.8 ± 0.5	481 ± 152	1E19
A3	829	20	0	2.8 ± 0.5	502 ± 150	1E19
A4	829	60	0	6.9 ± 0.5	510 ± 126	1E19
A5	829	120	0	10.3 ± 0.5	515 ± 63	1E19
A6	829	0	120	4.8 ± 0.5	65 ± 2	3E20
A7	829	5	115	4.9 ± 0.5	75 ± 2	3E20
A8	829	20	100	4.6 ± 0.5	153 ± 6	2E20
A9	829	60	60	4.9 ± 0.5	548 ± 138	1E19

In Table 2.1, the recipes and the results they obtained are given. From recipe A1 to A5, although the drive-in under O_2 ambient duration increases, the diffused regions' sheet resistance and surface concentration are similar. Figure 2.3.a and Figure 2.3.b illustrate that during the drive-in, P diffusion is blocked due to the oxidation of Si interstitials and probably the free P atoms on the atomic scale even if the SiO_2 thickness is lower than the equilibrium thickness. However, O_2 is not the only restricting mechanism of P diffusion into Si as it is illustrated in Figure 2.3.c. If the

SiO_2 thickness is larger than the equilibrium thickness, the Si interstitials cannot reach the PSG layer and form free P atoms. This situation is observed in recipe A9. When recipes A5 and A9 are compared, the same sheet resistances and surface concentrations are seen for both recipes. An additional drive-in under N_2 for recipe A9 does not change the results because of the thick SiO_2 layer grown during the first drive-in step under O_2 for 60 minutes.

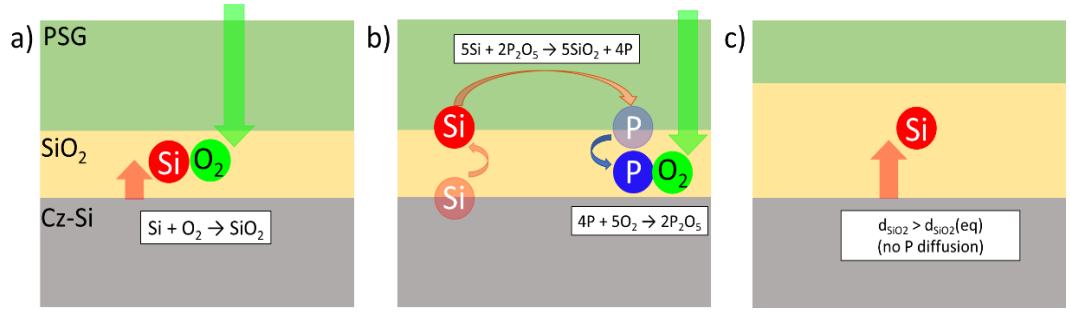

Figure 2.3. Blockage of P diffusion during O_2 drive-in due to a) oxidation of Si interstitials, b) oxidation of free P atoms and c) thick SiO_2 interlayer

2.3 Recombination

In Figure 2.4, the energy band diagram of the Si semiconductor is shown. When the semiconductor absorbs light, the electron in the valence band is excited to the conduction band and leaves a hole behind at the valence band, which acts as a positively charged particle. This excited electron and the empty space in the valence band are called as electron-hole pair. A certain amount of time passes before the electron loses energy and recombines with the hole. The duration between the excitation and recombination is called as minority carrier lifetime (τ_n or τ_p). The lifetime of the carriers depends on how many recombination active sites exist at the surface or bulk of the semiconductor. There are three types of recombination in single-crystal semiconductors: radiative, Auger and Shockley-Read-Hall (SRH).

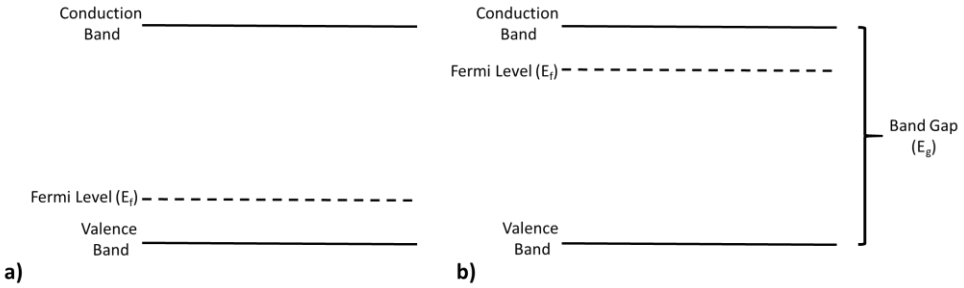

Figure 2.4. Energy band diagram of a) p-type Si, b) n-type Si

2.3.1 Radiative Recombination

The radiation recombination, which is also called band-to-band recombination, is the the inverse of electron excitation. Electron combines with the hole and emits a photon with an energy similar to the Si bandgap. This type of recombination is not a dominant mechanism in Si solar cells because Si is an indirect bandgap material. The schematic of the radiative recombination is shown in Figure 2.5.

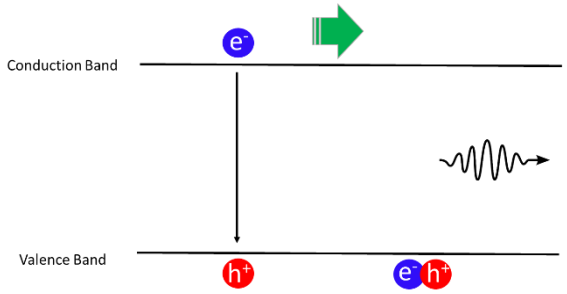

Figure 2.5. The schematic of radiative recombination.

2.3.2 Auger Recombination

Auger recombination is caused mainly due to the high dopant concentration or injection level. In the emitter, a region so-called dead layer, which has a dopant concentration above 1E20 cm^{-3}, suffers from this type of recombination. Three charge carriers are involved. Excess energy is transferred into an electron (eeh

process) or hole (ehh process). This electron and hole then thermalize back down to its original band edge. The schematic of the Auger recombination is shown in Figure 2.6.

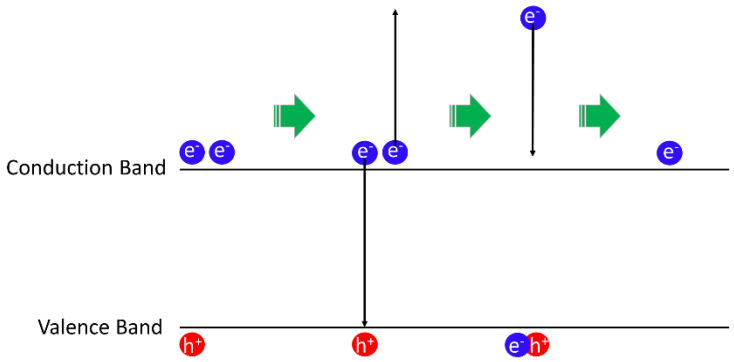

Figure 2.6. The schematic of Auger recombination.

2.3.3 Shockley-Read-Hall Recombination

Defect and trap levels in the band gap of the semiconductor mainly cause Shockley-Read-Hall (SRH) recombination. Inorganic and organic impurities are introduced in bulk intentionally (doping) or unintentionally during crystal growth and fabrication processes. First, electrons in the conduction band release energy and drops to an extra level in the forbidden gap. Then, electrons release more energy, drop the valence band, and recombine with holes. The schematic of the SRH recombination is shown in Figure 2.7.

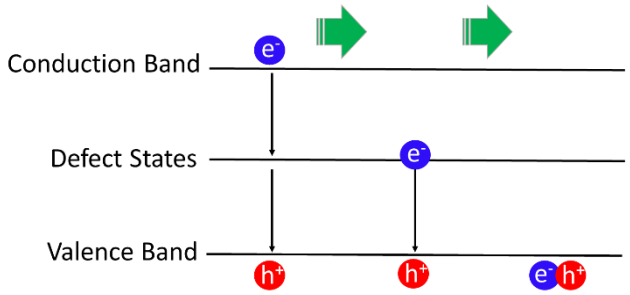

Figure 2.7. The schematic of SRH recombination.

2.4 Low-Temperature Annealing

Low-temperature annealing (LTA) is a process of annealing the emitter before or after the SiN_x deposition. LTA can be performed with a rapid thermal processing (RTP) tool for a very short time or in a tube furnace for a long time. The process is called as LTA because the annealing does not affect the active P concentration, which means the temperature is below the diffusion temperature. According to Shirazi et al., the LTA process dissolves electrically inactive P in the emitter, which is formed due to the rapid cooling down at the end of the diffusion process [9]. They demonstrated that depending on the inactive P in the emitter, reductions in the saturation current density of the emitter ($J_{0,e}$) are observed without any significant changes in the sheet resistance. In addition, it is known that the right amount of H in bulk and the surface helps to increase the passivation. However, an excess amount of H or lack of H causes deterioration of passivation. During the LTA process (≥400°C) after SiN_x deposition, H in the SiN_x layer is released [10]. J. Yoo et al. suggest that there is an optimized condition for the gas ratio of (NH3)/(SiH4+NH3) and annealing temperature to be maintained to obtain the highest lifetime values [11]. In Figure 2.8, for an annealing temperature of 800°C, the gas ratio is found to be 0.57.

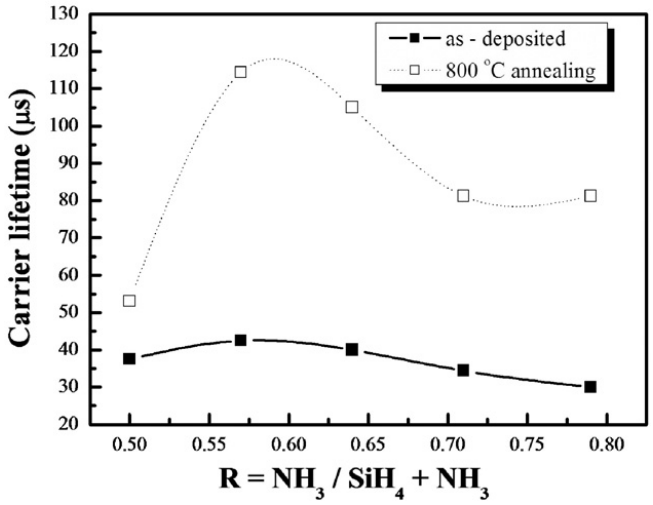

Figure 2.8. Effective carrier lifetime of as-deposited and annealed (at 800°C) SiNx films with different gas ratios (R) [11].

At an optimized condition, Sharma et al. show that by applying an LTA process, higher V_{oc} and J_{sc} values on n-PERT solar cells are obtained [12]. Also, the FF of the cell can be increased due to the passivation of crystallographic defects and gettering of metal impurities on the cast-mono crystalline wafers by an LTA treatment [13]. In addition, C. Sen et al. demonstrate that a pre-firing annealing process helps suppress light and elevated temperature-induced degradation (LeTID) on p-type mc-Si wafers [14]. They show that the degradation at the maximum degradation point, 40% less degradation, is observed for the annealed samples.

2.5 Thermal Oxidation

Thermal oxidation is one of the techniques that is used for passivating the Si surface with SiO_2. The main difference is that an oxidizing agent diffuses and reacts with the material itself. In the case of Si, O_2 diffuses and reacts with the Si atoms. Since Si atoms in bulk are bonded, it is impossible to grow SiO_2 in two lateral directions. The only way is to grow outside of the wafer. Si can be thermally oxidized by dry O_2 or water vapor (wet oxidation) by reactions shown in Eq.14 and Eq.15, respectively.

The oxidation rate is much higher with water vapor, so it is preferred to grow SiO_2 films thicker than 0.2 μm [15].

$$Si + H_2O \rightarrow SiO_2 + H_2 \quad \text{Eq.14}$$

$$Si + O_2 \rightarrow SiO_2 \quad \text{Eq.15}$$

Wet oxidation is preferred to grow thick SiO_2 films, but due to the fast oxidation, more dangling bonds are left unsaturated, which behave as recombination centers. Dry oxide is denser, cleaner and more controlled than wet oxide and saturates the dangling bonds at the Si surface better [16]. In this study, the passivation of the Si surface is the key goal. Thus, the thin dry oxide is enough the saturate the dangling bond at the surface.

The deal-Grove model describes the kinetics of the growth mechanism [deal-grove-ref]. According to the model, the required time (τ) for growing an oxide with a certain thickness (x_{ox}) on a bare Si surface at a constant temperature is:

$$\tau = \frac{x_{ox}}{B/A} + \frac{x_{ox}^2}{B} \quad \text{Eq.16}$$

where the constants A and B relate to the properties of the reaction and the oxide layer, respectively.

CHAPTER 3

FABRICATION OF SOLAR CELL

3.1 PERC Cell Fabrication

To observe the real performance of the optimized emitters, PERC solar cells are fabricated in this study. In this section, details about the process flows are described.

3.1.1 Properties and Fabrication of Si Wafer

PERC cells are currently the dominant cell structure in the PV market due to their high efficiency, low cost and simplicity in fabrication. P-type (B-doped) Czochralski-grown Si wafers (Cz-Si) are preferred since the segregation coefficient (k_o) of B is 0.8, which means that a slight change in the resistivity throughout the ingot is observed [17]. To fabricate p-type wafers, B is usually used as a base dopant. However, in the case of gallium (Ga), the segregation coefficient is 0.008 [18], so significant changes in the ingot are observed and industrial point of view; this is not a desirable situation. Moreover, by comparing with n-type wafers, B-doped p-type wafers have the advantage of low cost. However, B-doped p-type wafers suffer from light-induced degradation (LID) due to boron-oxygen (BO) complexes and light and elevated temperature-induced degradation (LeTID). Also, they are sensitive to metallic impurities more than n-type wafers. It is possible to partially eliminate LID, LeTID and metallic impurities by a gettering process like phosphorus diffusion [19], [20]. After the growth of the Si ingot, a wire saw is used to slice ingot into wafers.

3.1.2 Texturing and Cleaning

After Si ingots are grown, they are sliced into Si wafers with a thickness of around 180-200 μm by a wire saw. Due to the nature of the process, saw damages on the surface exist and the resulting surface is reflective. The wafers at this stage are called-as as-cut wafers. To remove saw damages and absorb more light, the surface structuring process so-called texturing is applied.

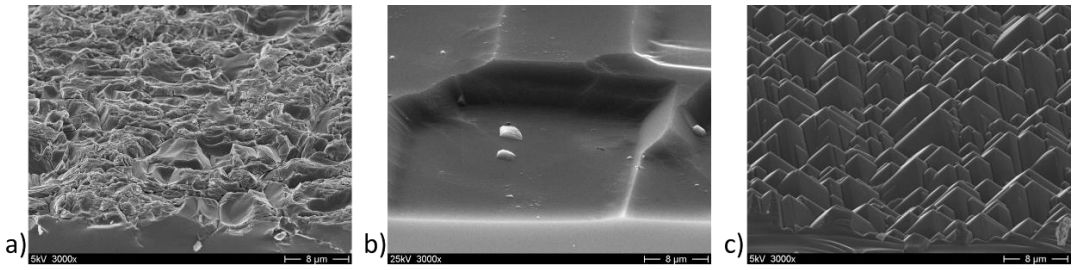

Figure 3.1. SEM images of the surfaces a) as-cut (saw damaged), b) saw damage etched and c) random pyramidal textured [21]

In Figure 3.1.a, scanning electron microscopy (SEM) image of a saw damage surface is shown. When slicing ingots into wafers, the surface becomes rough and contains impurities. In ODTU-GÜNAM Photovoltaic Line (GPVL), surface structuring is done by the RENA Batchtex device. First, as-cut wafers go into a bath with a mixture of DI Water and KOH. Saw damages due to the slicing process are removed with a diluted KOH solution. These saw-damaged removed wafers are called as saw damage etched (SDE) wafers and the surface of the wafers are nearly polished which is shown in Figure 3.1.b. After saw damage removal process, the wafers go into the process bath. This bath contains a mixture of deionized (DI) water, KOH and monoTEX additive. The process is based on the difference in etch rate between the faces. Etch rate of {100} and {110} faces are much higher than {111} face. Due to this difference, the pyramidal shape is formed on the surface, as illustrated in Figure 3.1.c.

Figure 3.2 explains the logic behind this type of surface structuring. When the light arrives at the surface, there are two options: Absorb or reflect. In the case a), the light is reflected. If the surface is polished, as in SDE wafers, the light has only one chance to get absorbed by the wafer. If the surface is textured, the light can also reflect, but now it has a second chance of getting absorbed by the wafer. The texturing process can reduce the amount of reflection from ~30% to ~10%. In the case b), light is absorbed by the wafer. Finally, in the case c), the light is either transmitted or reflected at the rear surface. High energy photons are absorbed easily in the Si bulk closer to the front surface. However, low-energy photons get absorbed closer to the rear surface. Therefore, if the light is not absorbed, it can be reflected back at the rear surface and had another opportunity to be absorbed by the Si. Textured surface changes the light's direction and when it reaches the back surface, it is not perpendicular. So, the light can be reflected back into Si [22].

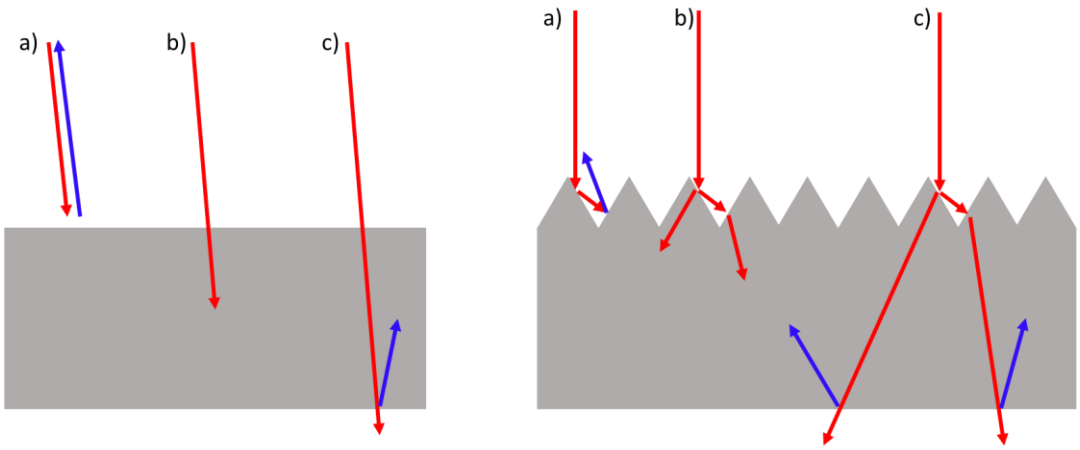

Figure 3.2. Effect of texturing process on light absorption.

After the texturing process, the O_3 cleaning process is realized in another bath to remove inorganic and organic impurities on the wafers. A thin ozone-oxide layer is grown on the wafers' surface, so a small amount of Si is also removed. To remove the undesired ozone-oxide layer, wafers go into an HF bath. After rinsing the wafers in deionized water (DI water) and drying them in a hot N_2 environment, the wafers are ready for the doping process. The final structure at the end of the texturing process is shown in Figure 3.3.

Figure 3.3. The schematic of the Si wafer after the texturing process.

3.1.3 Doping

The light excites an electron from the valence band to the conduction band when absorbed by the semiconductor and an electron-hole pair is created. If these electron-hole pairs are not separated by a junction and collected after, the electron loses energy and recombines. By doing so, electrons generate heat or light depending on the semiconductor's bandgap structure. In photovoltaics, it is desired to separate and collect electron-hole pairs effectively to generate electricity. To do that, a p-n junction is introduced in the device to create an embedded electric field. In the absence of a junction, carriers do not have a defined direction, so they move a certain distance at a constant velocity but in a random direction [23]. In the presence of a p-n junction, due to drift current, carriers have a net direction depending on the charge of the carrier. In PERC cells, B-doped p-type wafers are used. Therefore, the n+ emitter region is formed on the front side of the wafer to create a p-n junction mostly either by $POCl_3$ diffusion, P ion implantation, PH_3 Diffusion or atmospheric pressured chemical vapor deposition (APCVD) deposited PSG. In ODTÜ-GÜNAM, atmospheric pressure $POCl_3$ diffusion is used due to the low costs, good stability, relative simplicity, and high throughput of the available production equipment [24]. Figure 3.4 shows the schematic of the process gas flows during the pre-deposition process. There are three mass flow controllers (MFC). MFC-1 controls the flow of N_2 carrier gas flow in the bubblers, while MFC-2 controls the flow of N_2, which is used for the carrier gas stream in the furnace. MFC-3 controls the O_2 flow, which is necessary for pre-deposition and drive-in steps. The gases from MFC-2 and MFC-3

are joined right after they leave MFCs. On the other hand, N_2 carrier gas flow from MFC-1 goes through the $POCl_3$ bubbler and $N_2/POCl_3$ mixture is come out of the bottle. Then, right before the furnace's inlet, the MFC-2 and MFC-3 are joined with the gas flow left from the $POCl_3$ bubbler.

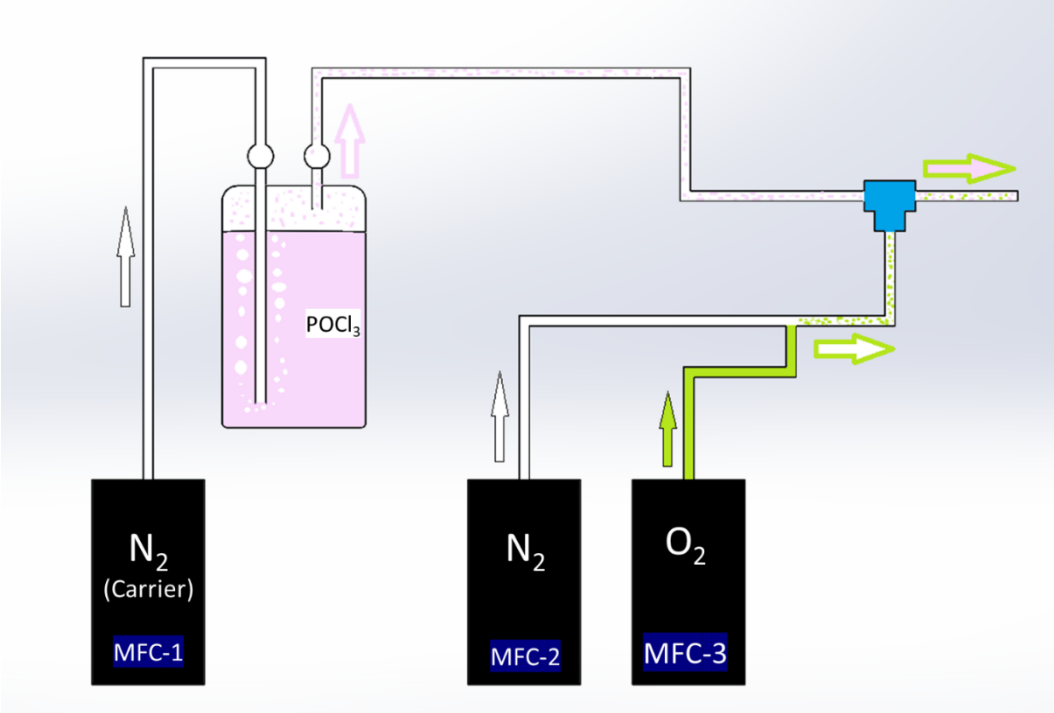

Figure 3.4. The schematic of the gas flows during the pre-deposition process.

To load the Si wafers into the diffusion furnace, a diffusion boat with 270 slots is used. Schematics of the boat and loaded wafers are shown later in section 4.1. After wafers are loaded into the boat and sent into the tube, the temperature is ramped up to pre-deposition conditions. O_2, N_2, and carrier N_2 gas flows are active during the pre-deposition. During this step, P_2O_5 is formed due to the reaction of $POCl_3$ and O_2. Then, this P_2O_5 reacts with the SiO_2 on the Si surface and forms PSG, which acts as an infinite P source. At the end of the pre-deposition, the temperature is ramped up to the drive-in conditions. During the ramp-up and drive-in steps, the N_2 flow is always active, but depending on the application, O_2 flow is either active or not. Then, the temperature decreases to a temperature lower than 800°C and the samples are

removed from the furnace. More detailed information, literature reviews and chemical mechanism of the process were given in section 2.2. The current structure after the diffusion process is shown in Figure 3.5.

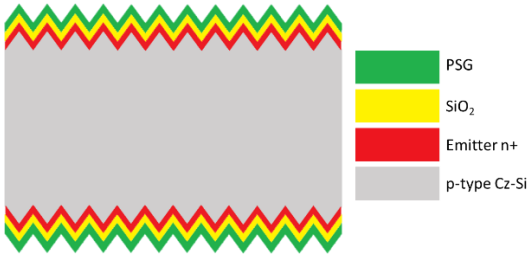

Figure 3.5. The schematic of the Si wafer after diffusion process.

3.1.4 Single Side Etching

The formation of the p-n junction is done by the $POCl_3$ diffusion process. However, as seen in Figure 3.5, both the front and rear surfaces have a diffused region. Electrons are collected at the n+ emitter region and holes from the p-type bulk region. If the emitter and bulk regions are not isolated, an alternative way for the electrons will exist and reduce the shunt resistance of the device. Thus, the FF of the cell will be decreased, which will cause low PCE. A single-side etching (SSE) process is applied to the wafers right after the diffusion process to overcome this problem. In addition, at the end of this process, the rear surface morphology is also changed. While etching the phosphorus diffused region from the rear side, the surface is polished in the process bath. Polish surface has higher electrical performance due to reduced surface area. It also has higher reflection than a textured surface which is necessary for back reflection of the non-absorbed light. This polishing increases the IR response of the device.

RENA Inpilot device is used for the SSE process. After the diffusion process, the samples are put on the device's rollers. The rollers turn and move the wafers from one bath to another. The main goal of the process is to protect the front side while the rear side of the wafers is etched and polished. In the process bath, the wafers' rear side is etched with the mixture of $HNO_3/HF/H_2SO_4$, while the front side is protected

with DI water. The final structure at the end of the SSE process is given in Figure 3.6.

Figure 3.6. The schematic of the Si wafer SSE process.

3.1.5 Dry Oxidation

The proper structure is formed on the Si wafers at the end of the SSE process. Emitter and bulk regions are isolated with a p-n junction and the electrons and holes can be separated effectively. However, preventing electron-hole pairs from recombination is now the primary concern. There are many reasons to cause recombination in solar cells. P diffused emitter is a highly recombinative region due to a high amount of dopant which causes Auger recombination. Also, because of the impurities and defects in the bulk and emitter, SRH recombination exists. Moreover, the surfaces of both sides of the wafer are highly recombinative regions due to dangling bonds.

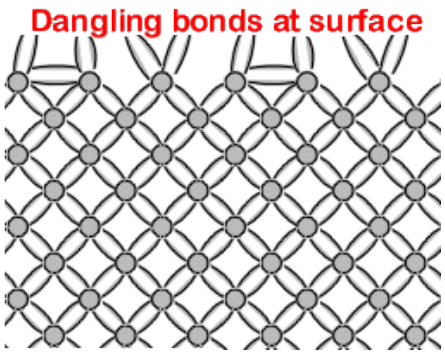

Figure 3.7. The schematic of the dangling bonds at surface [23]

In Figure 3.7, the crystal structure of a Si wafer is shown. At the surface, Si atoms have dangling bonds accepted as recombination centers. To saturate these bonds, surfaces should be passivated with dielectric layers. These layers should have the

capability to saturate the bonds at the surface, should not absorb any photon in the solar spectrum and should not create inversion at the surface.

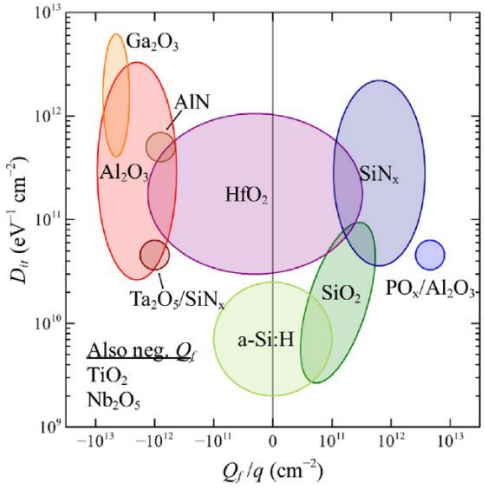

Figure 3.8. Q_f vs. D_{it} graph of commonly used dielectric materials in PV applications [25].

In Figure 3.8**,** some dielectric materials are shown. Generally, low interface defect density (D_{it}) and high fixed charge density (Q_f) are desired depending on the surface type and application. Thermally grown SiO_2 has already been shown as a good chemical passivator and has positive fixed charges, but the fixed charge density of the SiO_2 is low [26]. Also, it grows on both sides of the wafers. Low D_{it} of the layer is desired, but low positive fixed charge density does not exactly satisfy the requirements for both sides. Therefore, a low-temperature oxidation is applied after the SSE process to grow a very thin layer of SiO_2 on both sides of the wafer. In a tube furnace, the low-temperature oxidation process is realized at a temperature of 600°C for 40 minutes. Figure 3.9 shows the structure formed after oxidation. SiO_2 passivation effects on the emitter are later discussed in section 4.2.

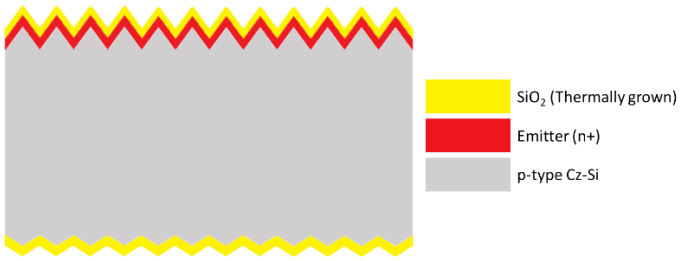

Figure 3.9. The schematic of the Si wafer after thermal oxidation process.

3.1.6 Al_2O_3 Deposition and Activation

Atomic layer deposition (ALD) is a method to deposit ultra-thin films in a precisely controlled way. Dielectric films are deposited layer by layer. In ODTÜ-GÜNAM facilities, to deposit Al_2O_3 on Si wafers, Solaytec ALD device is used. It has already been discussed that with the help of the p-n junction, electrons and holes are effectively separated from each other. At the rear side of the cell, holes are the majority carriers and the existence of electrons in that region will cause recombination. A dielectric layer with a negative fixed charge density is necessary to repel electrons from the rear surface. In Figure 3.8, it is shown that the Al_2O_3 layer has high negative fixed charge density. The mechanism of the deposition is shown in Figure 3.10. During the deposition, the wafer goes forward and backward repeatedly. Trimethylaluminum (TMA) is used as an Aluminum (Al) precursor and liquid DI water is used as an oxygen (O) precursor. When the wafer's rear side reaches the TMA processing compartment, a mono layer is formed on the surface. After that, the wafer moves and reaches the H_2O processing compartment. A chemical reaction between H_2O and the monolayer formed by TMA is realized. The product of this reaction is the requested Al_2O_3 dielectric layer. The repetition number of this process determines the thickness of the layer, or in other words, the number of monolayers determines the thickness.

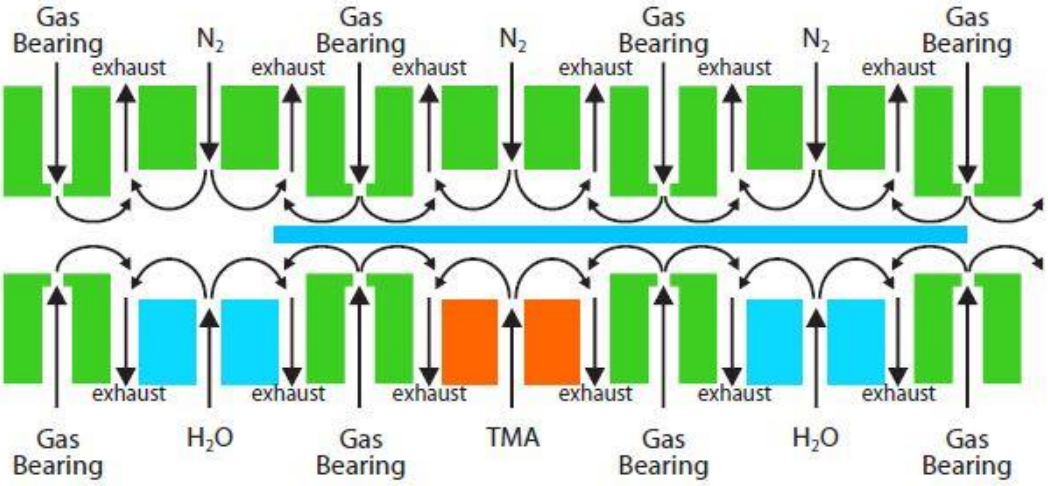

Figure 3.10. The schematic of the deposition of stoichiometric Al_2O_3

The deposited Al_2O_3 layer is not an active passivation layer. Also, Hydrogen (H) in the layer can cause blistering which leads to the degradation of the passivation [27]. Therefore, an activation annealing process is applied in a tube furnace. In ODTÜ-GÜNAM, this annealing process is applied at 425°C for 15 minutes under N_2 ambient and during the annealing process, the layer is activated and degassed. The structure after the deposition of the Al_2O_3 layer is illustrated in Figure 3.11.

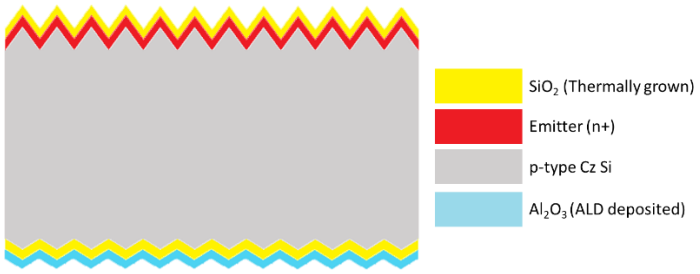

Figure 3.11. The schematic of the Si wafer after Al_2O_3 deposition.

3.1.7 ARC and Capping Layer Deposition

For the p-type rear surface passivation, SiO_2 and Al_2O_3 provide chemical passivation and field-effect passivation, respectively. To create field-effect passivation on the front side and enhance the chemical passivation effects of SiO_2, a plasma-enhanced chemical vapor deposition (PECVD) grown silicon nitride (SiN_x) layer is used. In Figure 3.8, it is shown that the SiN_x layer has positive fixed charge density and the amount of the fixed charge depends on the stoichiometry of the layer. Also, the SiN_x layer act as an anti-reflective coating (ARC).

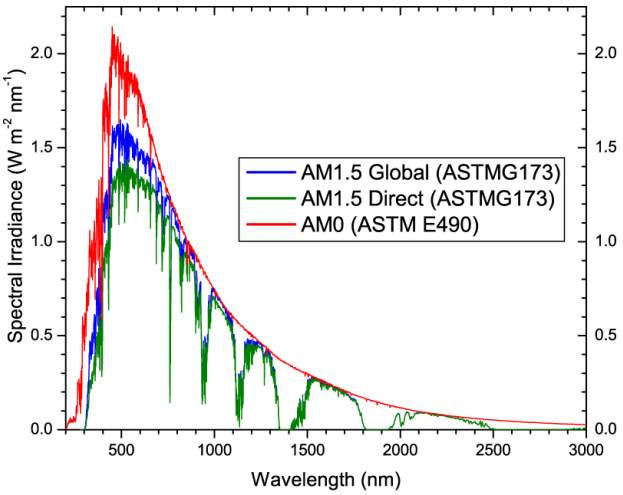

Figure 3.12. Standard Solar Spectra for space and terrestrial use.

The spectrum of the sunlight is shown in Figure 3.12. The peak of the spectrum is around 600 nm, which means that the maximum intensity of sunlight coming from the sun has a wavelength of around 600 nm. To absorb maximum sunlight from this portion of the spectrum; refractive index, stoichiometry and the thickness of the layer should be optimized.

Another SiNx layer is optimized for the rear side of the wafer. At the front side, the main goals for the layer are passivating the n+ emitter and absorbing sunlight as much as possible. However, at the rear side, the SiN_x layer is used as a capping layer for Al_2O_3 and a back reflector for the non-absorbed light. The Al_2O_3 layer is an ultrathin layer and is sensitive to degradation during the contact firing process. SiN_x

layer also acts as an H source and improves the passivation quality at the rear side. In addition, the bandgap of Si is 1.12 eV and Si can absorb sunlight with a lower wavelength than 1100 nm. Especially, after the 950 nm wavelength, the absorption coefficient is reduced dramatically and the 950-1100 nm portion of the spectrum can be absorbed closer to the rear surface. If the light is not absorbed, with an optimized SiN_x layer, light can be reflected back into Si and have a second chance to be absorbed. The structure formed after the deposition of the SiN_x layers is illustrated in Figure 3.13.

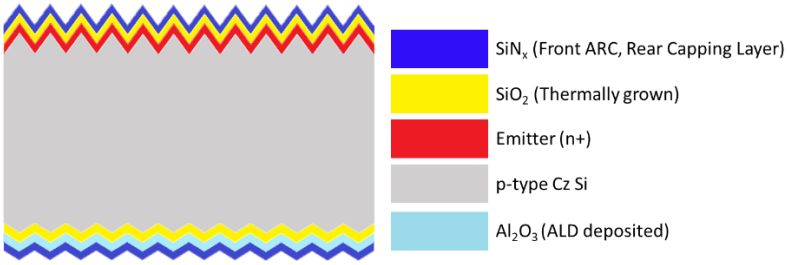

Figure 3.13. The schematic of the Si wafer after SiNx deposition.

3.1.8 Laser Ablation for Local Contact Opening

For some solar cells like IBC, n-PERT or TOPCon, the back surface field or front surface field is formed before the passivation layers' deposition; generally, P or B diffusions are preferred. For PERC cells, Al is used as BSF due to its low cost and simplicity. However, unlike standard Al-BSF solar cells, the rear side of the PERC solar cell is aimed to be passivated because BSF regions created with Al are highly recombinative. However, the Al paste used to form BSF regions is not able to diffuse through the deposited SiNx layer. Therefore, local openings on the SiNx layer at the rear side are required. To do that, a laser process so-called laser ablation is applied on the rear side. These openings are called as laser contact opening (LCO) and after the metallization/firing process, Al paste fills these LCOs and create Si-Al alloys which help the diffusion of Al atoms into Si. The created structure at the end of the laser ablation process is shown in Figure 3.14.

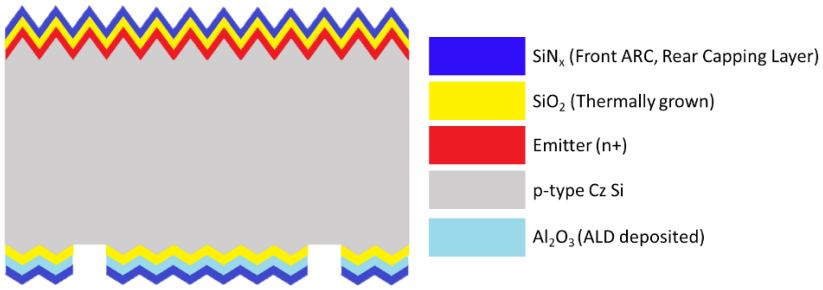

Figure 3.14. The schematic of the Si wafer after LCO.

3.1.9 Contact Formation

Figure 3.14 illustrate the final structure before the contact formation. When the light comes, it will excite an electron and create electron-hole pair. Due to p-n junction, electrons and holes can be separated from each other (electrons gathered on the emitter side, holes gathered on the bulk) and passivation of both surfaces will help increase the carriers' lifetime. Now, it is required to collect carriers via metal contacts to send them into an external circuit.

In the emitter region, an Ag paste with a firing-through capability collects electrons on the front side. Fire through means that the paste can diffuse through the SiNx layer and get direct contact with the emitter. For the rear side, Al paste is used to form BSF regions and contact. First, Al paste is screen printed on the rear side and went into the dryer. After that, front-side screen-printing metallization is done by a silver paste with an optimized finger and busbar numbers and then goes into the dryer. The structure formed after the metallization process is shown in Figure 3.15.

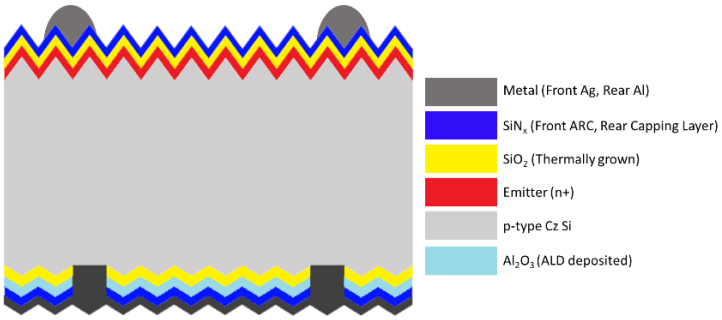

Figure 3.15. The schematic of the Si wafer after metallization.

After the metallization process, a fast-firing process is applied to the wafers to complete the contact formation and activation of the passivation layers. Before the firing process, Ag paste is just printed and has no contact with the emitter region and Al atoms at the LCO have not formed a BSF region yet. The wafers are placed on the belt, constantly moving at a defined speed. The firing furnace has six different zones with different temperatures to create a suitable temperature profile. The firing process bonds silver to Si at the front and forms BSF regions at the rear side with the help of Si-Al alloys. Al paste fills these LCOs and creates Si-Al alloys which help the diffusion of Al atoms into Si. Figure 3.16 illustrates an SEM image of the formed Al-BSF region.

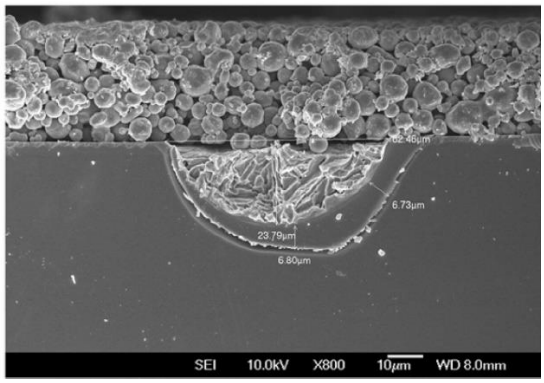

Figure 3.16. SEM image of the LCO after contact formation [28].

The PERC cell fabrication process is completed at the end of the firing process. After the firing process, cells were characterized by current-voltage (I-V) measurements with a class AAA solar simulator. The complete structure of the cell is shown in Figure 3.17.

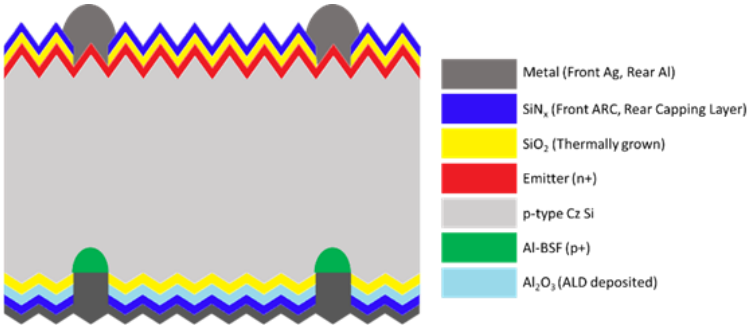

Figure 3.17. The schematic of the Si solar cell after contact formation.

3.2 Lifetime Samples

This section gives information about the process flow for lifetime samples. Lifetime samples are necessary to extract the $J_{0,e}$, bulk lifetime (τ_{bulk}) and implied open circuit voltage (iV_{oc}). For the symmetrical emitter samples, the different $POCl_3$ diffusion process is applied to the wafers after texturing and cleaning processes. However, instead of an SSE process, the rear side emitter is kept and only HF dipping is applied on the wafers after the diffusion process to remove PSG/SiO_2 on the surfaces. Then, the passivation layers are deposited on both sides of the wafer. After that, wafers are laser-cut into nine pieces by a laser marker for fast-firing process optimizations. The schematic of the fabrication of the lifetime samples is illustrated in Figure 3.18.

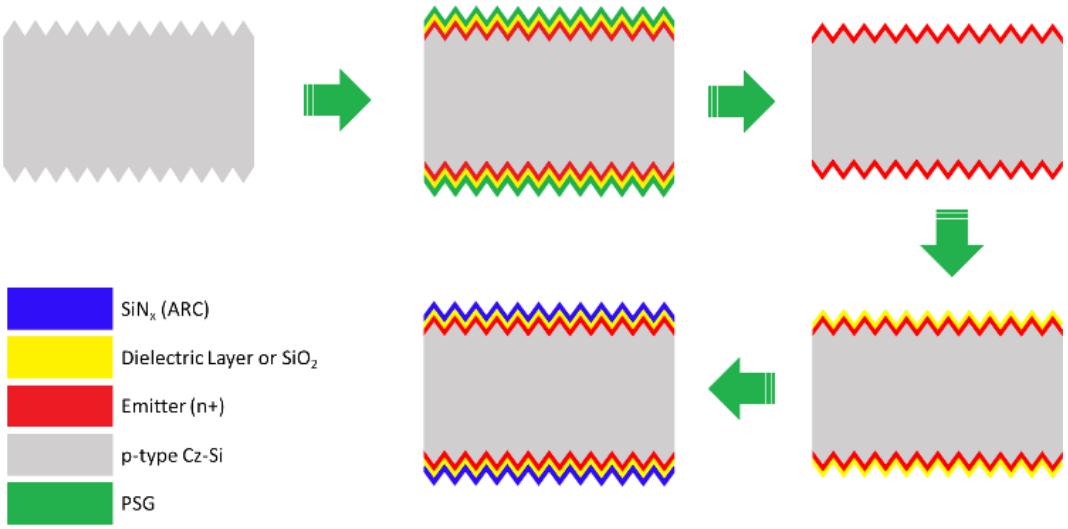

Figure 3.18. The schematic of the fabrication of symmetrical emitter samples

3.3 Measurement Methods

3.3.1 4-Point-Probe

L.B. Valdes proposed the method in 1954, aiming to measure the resistivity of both sides of the p-n junction [29]. Using a 4-point-probe (4PP), the resistivity of different layers and bulk semiconductor materials can be measured [30].

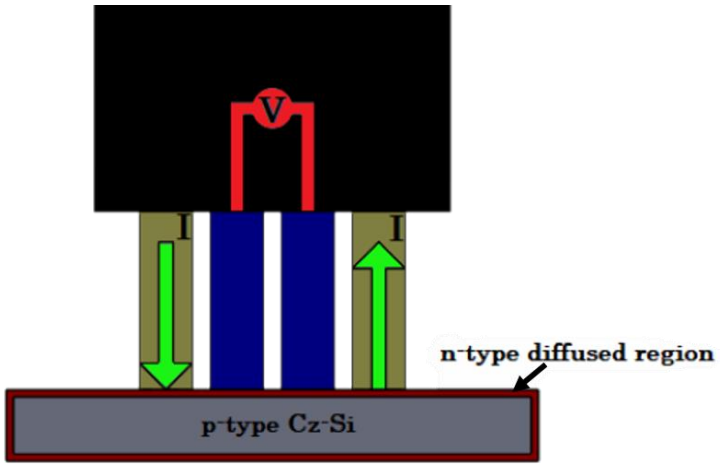

Figure 3.19. The schematic of 4PP measurement

In Figure 3.19, the working principles of a four-point probe are shown. Current (I) flows through the outer probes, while the inner probes measure the floating potential (V). During the optimization studies, PVTOOLS TLM-SCAN four-point probe is used after doping to measure sheet resistances of emitters. The samples are p-type Cz-Si wafers with a size of 156.75 mm x 156.75 mm. Measurements are taken from 25 different points on every sample to determine the uniformity of the diffusion process. The non-uniformity of the wafers is specified with a standard deviation (±).

3.3.2 Electrochemical Capacitance-Voltage

The electrochemical capacitance-voltage (ECV) method is widely used to measure the active dopant profile of specimens. After every doping process, Wafer Profiler CVP21 was used for the ECV measurements. The schematic of the ECV measurement is shown in Figure 3.20. Ammonium bifluoride (NH_4HF_2) is an electrolyte that does not directly etch the Si under no electricity conditions. For p-type surfaces, holes are the majority carriers which is essential because to etch Si; four valence electrons recombine with holes and the remaining positively charged Si+4 core atom is then diffused through the negatively charged electrolyte. However, in the case of n-type Si, holes are minority carriers. Therefore, n-type surfaces cannot be etched in the same way as p-type surfaces. Two possible solutions exist. First, etch voltage can be increased so that the Schottky interface goes into a breakdown condition, creating a very huge etch current. However, the user cannot control this voltage, and the company does not recommend this method. Second, due to the lack of holes in the n-type semiconductors, electrons are excited by photons. With the help of the Schottky depletion layer on the semiconductor surface, holes move through the semiconductor surface and electrons move through the semiconductor bulk. Then, created holes can release valency electrons by recombination. Like in the p-type material, if all the valency electrons can be removed, then the positively charged core Si atom can diffuse through electrolyte fluid.

The user manual provided by the company and other studies in the literature suggest that sheet resistance calculated by ECV should be corrected by 4PP. This can be done by calibrating the device with a bulk wafer that has the same surface morphology as real samples to find out the surface roughness or changing the surface roughness value to get the same sheet resistance value with 4PP [31], [32].

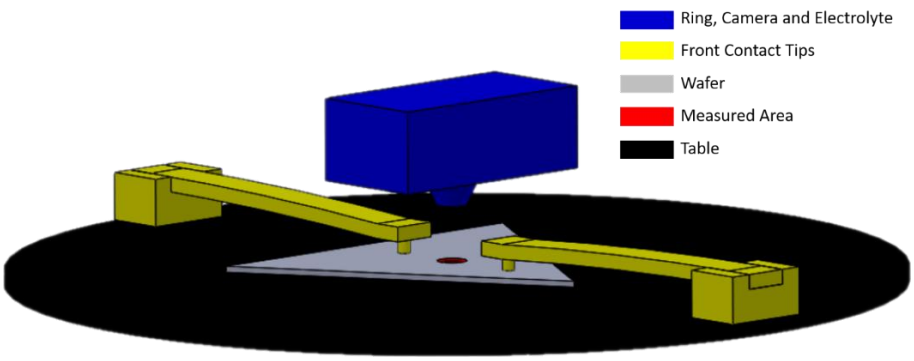

Figure 3.20. The schematic of ECV measurement

3.3.3 Sinton WCT120TS Lifetime Tester

Sinton WCT-120 and Sinton WCT-120TS are used for quasi-steady-state photoconductance (QSSPC) measurements [33]. With the help of an RF coil and an IR pass-filtered xenon flash lamp, the instrument measures the samples' effective carrier lifetime (τ_{eff}). The instrument is an ideal and accepted device in the literature

to measure dopant diffusion and passivation quality of that diffused region. The schematic of the Sinton WCT-120TS device can be seen in Figure 3.21.

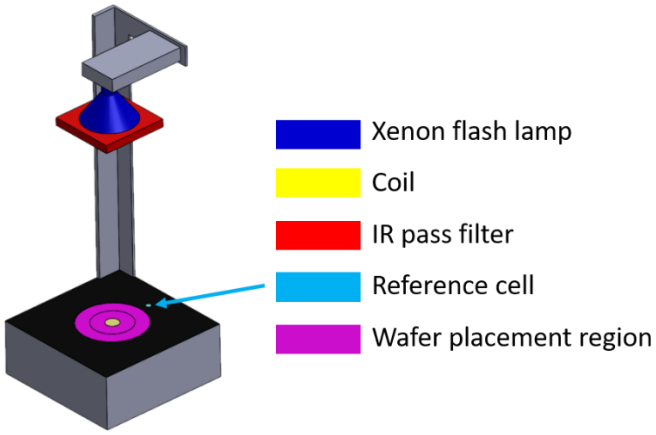

Figure 3.21. The schematic of Sinton WCT-120TS device

Carrier lifetime is the time between the generation and the recombination of the minority carrier. τeff, which is measured by the photoconductance method, represents carrier lifetime affected by all recombination channels existing in the wafer. Since surfaces are passivated during the high-temperature phosphorus diffusion process by the PSG layer, measured τ_{eff} after the diffusion step gives a strong idea about the final cell lifetime. If both the front and the rear surface of the wafer are diffused, then the following expression shows the effective lifetime of the sample:

$$\frac{1}{\tau_{eff}} - \frac{1}{\tau_{Auger}} = \frac{1}{\tau_{SRH}} + [J_{0,e(front)} + J_{0,e(rear)}]\left(\frac{N_A + \Delta n}{qWn_i^2}\right) \qquad \text{Eq.17}$$

Here, elementary charge (q) equals 1.602E-19 C and n_i equals 8.6E9 cm^{-3} at 25°C. The user must know that W represents wafer thickness and N_A is the number of acceptor atoms, which in this case is base doping. Δn is the injection level at which the device provides the data. τ_{Auger} and τ_{SRH} are Auger recombination lifetime and SRH recombination lifetime, respectfully. $J_{0,e(front)}$ and $J_{0,e(rear)}$ represent the emitter's saturation current density, which characterizes the emitter region. Auger recombination is the dominant recombination channel in the emitter region and τ_{Auger}

strongly depends on the Δn. The software provides the plot of inverse auger corrected lifetime vs. injection level, which gives the information of $J_{0,e}$.

3.3.4 Transfer Length Method (TLM)

The transfer length method (TLM) is widely used to calculate the contact resistivity between metal and semiconductor ohmic structures. In the case of industrial PERC cells, instead of a spreading structure, finished solar cells with equidistant contacts are cut into stripes to isolate the fingers. The method proposes to measure the voltage drop between all the permutations for the array of contacts. Then, by using the least squares approach, a linear fit is obtained and the sheet resistance of the semiconductor (R_{sheet}) is the slope of the fit and the contact resistance (R_c) is the interception of the fit and the resistance axis[34]. In this study, the PVTOOLS TLM-SCAN device is used to measure contact resistivity and the schematic of equidistant TLM stripe structure can be seen in Figure 3.22.

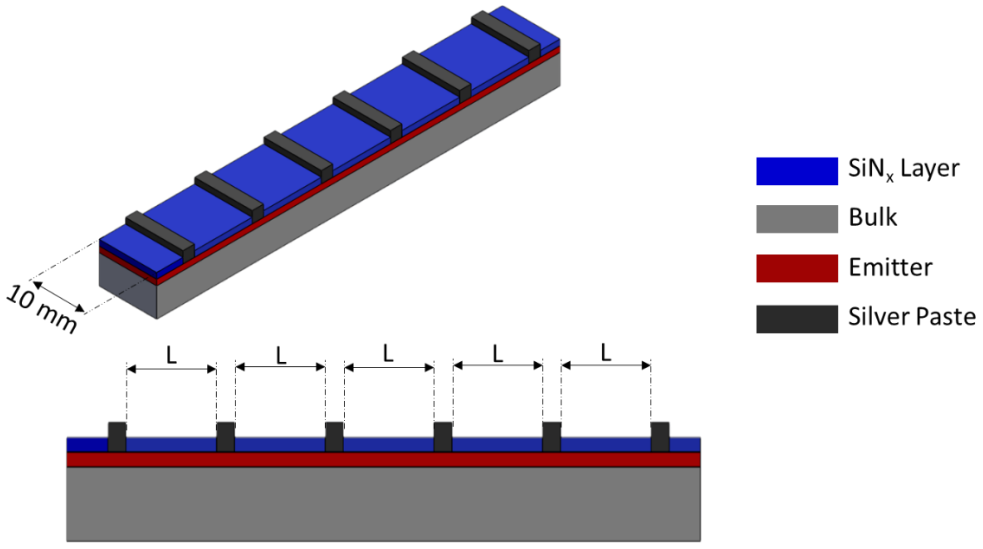

Figure 3.22. The schematic of a TLM stripe

3.3.5 IV Measurement

The current and voltage (I-V) properties of a photovoltaic (PV) cell show the cell's solar energy conversion capacity and efficiency. One can determine the cell's output performance by knowing its I-V characteristics. Some important parameters should be known when characterizing the cell performance. The first one is V_{oc}, which is the voltage across the cell when no electrical load is applied. The second parameter is I_{sc}, which is the current value when the voltage across the cell is zero. The third parameter is the FF, which shows the recombination losses at the junction and resistive losses. The slope of the curve at J_{sc} gives information about the shunt resistance and the slope of the curve at V_{oc} provides information about the series resistances. The curve at J_{sc} should be as horizontal and the curve at the V_{oc} should be as vertical as possible for an efficient solar cell.

After designed PERC cells were produced, Mondragon Assembly Photovoltaic Cell Tester and Sorter was used. The schematic of the measurement is shown in Figure 3.23. During the measurement, probes contact the cell from the front busbars and rear Al metallized area.

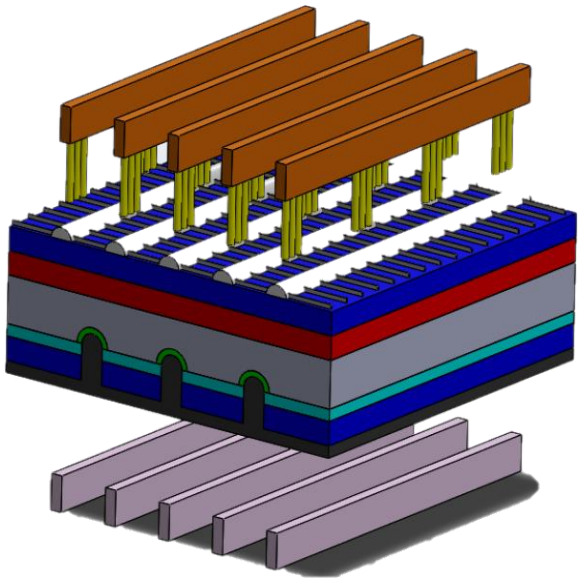

Figure 3.23. The schematic of IV measurement

CHAPTER 4

RESULTS AND DISCUSSION

4.1 Optimization of the Process Conditions

The resulting emitter profile depends on parameters like temperature, duration, gas ratios, configuration and position of the wafers. The amount of P in the PSG layer depends on gas ratios between $POCl_3$ carried by N_2 and O_2 while increasing temperature or duration helps more P atoms diffuse from PSG to Si wafer and obtain deeper profiles. Also, the configuration and positioning of the wafers affect the flow in the tube, so it is critical to optimize the positions and number of wafers used in the process. The reason is that in atmospheric diffusion furnaces, uniformity and amount of dopant diffused into the wafer highly depend on the amount of wafer and the flow in the tube. DG Plasma diffusion furnace has a boat with 270 slots, which means 270 wafers can be processed symmetrically or 540 wafers can be processed single side if two wafers are put on the same slot back-to-back. Due to the lack of dummy wafers during the experiments, the so-called full-boat doping processes in Figure 4.1a are held on with 200 wafers. In addition, the so-called 3-Spacing doping processes in Figure 4.1b with 68 wafers are carried out to realize the diffusion process with fewer samples. In the figure, red wafers represent the samples used for 4PP measurements while blue samples are used for lifetime measurements. In

addition, gray wafers represent the dummy wafers used to fill the entire boat to provide uniform gas flow.

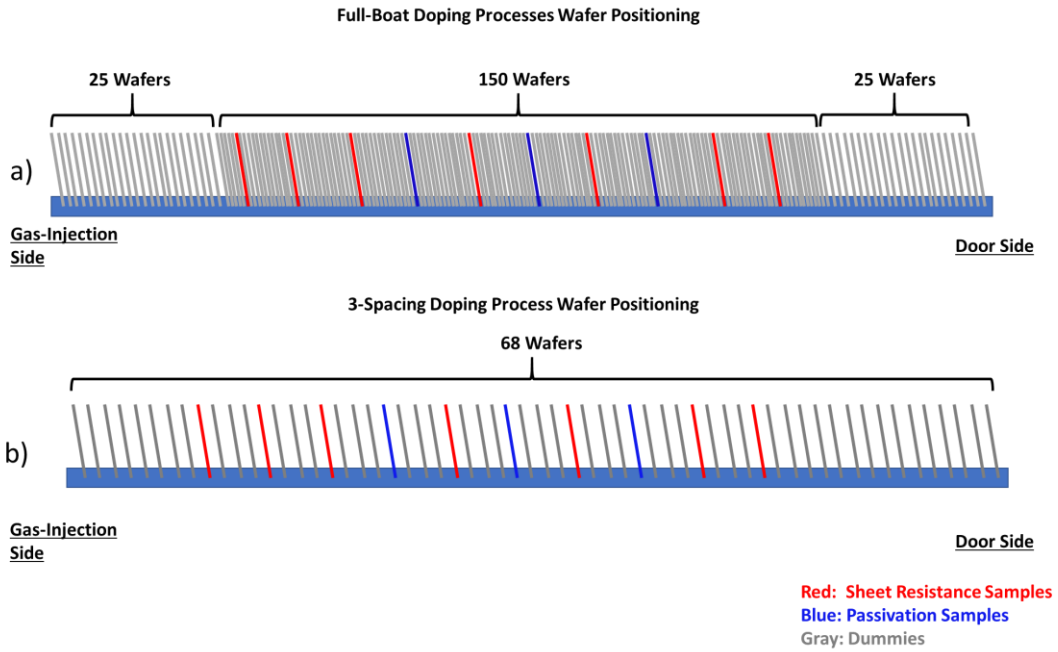

Figure 4.1. Configuration and positioning of the wafers a) Full-boat b) 3-spacing

Figure 4.2 shows the active dopant profiles and resulting sheet resistance values of the same recipe with full boat and 3-spacing boat configuration. Also, the wafers' sheet resistance and non-uniformity values are given in

Figure 4.3.

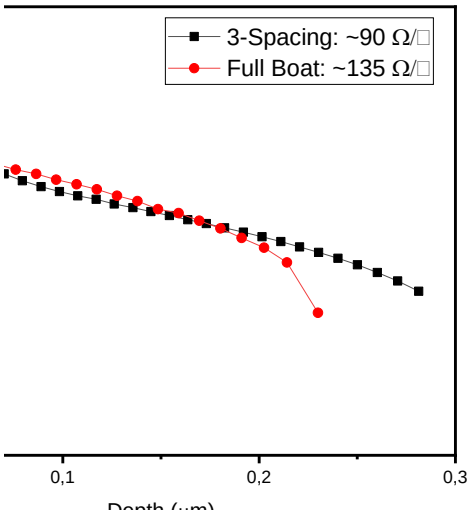

Figure 4.2. Active dopant profile of 3-spacing and full-boat configuration of the same diffusion recipe

The sheet resistances and uniformity values of the two groups of samples are given in Figure 4.3. For “Full Boat” processes, the reduction in the active dopants is observed due to the changes in the gas flow and the increase in the number of wafers. Also, the uniformity problem arose, possibly due to the smaller distance between the wafers.

Figure 4.3. Sheet resistance and non-uniformity values of 3-spacing and full-boat configuration of the same diffusion recipe

4.2 Optimization of the Emitter Profile

In the literature, the mechanism of the $POCl_3$ emitter has already been studied in detail. In this study, a set of experiments was conducted for optimization study. In Figure 4.4, the process flow is shown. After texturing and cleaning processes, six different diffusion processes were carried out. After HF dipping to remove the PSG layer on the symmetrically diffused emitter samples, passivation layers were deposited on both sides. Then, wafers were laser-cut into nine pieces and a firing study was held on.

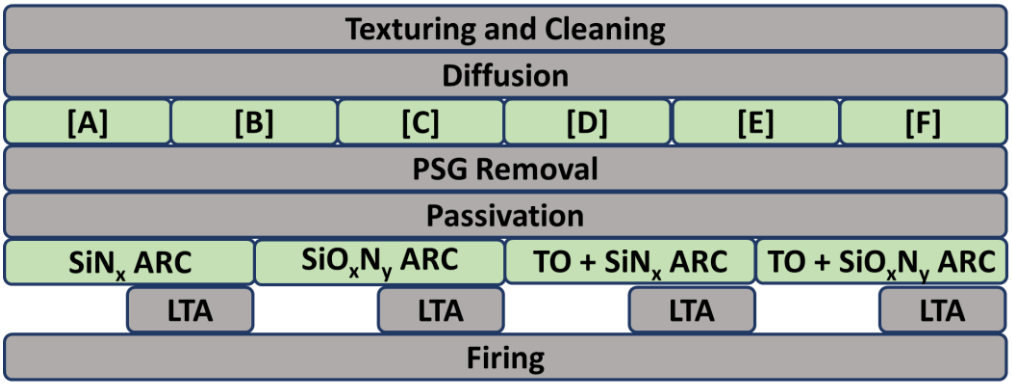

Figure 4.4. Process flow of the fabricated symmetrical 6 different ([A]-[F]) emitter samples

Details of the diffusion recipes are shown in Figure 4.5. The recipe [A] was kept as the control group. As mentioned before in section 2.2, to see the effect of drive-in conditions, the recipe [B], [C], [D] and [E] all have the same pre-deposition conditions. $POCl_3/O_2$ gas flow during the deposition was kept at 1000/1400 sccm and temperature and time were set as 780°C and 25 minutes, respectively. To observe how many carriers diffused into the wafer at the pre-deposition step, recipe [B] just underwent pre-deposition, and samples were taken out of the furnace. For recipe [C], ramp-up, drive-in and cool down steps were realized under N_2 ambient, meaning that Si interstitials are free to move through the PSG layer and create free P atoms. The expectation is to get a heavily doped emitter. For recipe [D], while the ramp-up and

cool-down steps were realized under N_2 ambient, the drive-in step was carried out under O_2 ambient. Si interstitials are free to move through the PSG in ramp-up and cool-down steps. However, at the drive-in step, O_2 oxidizes the Si interstitials and blocks the diffusion of P atoms into the Si wafer. We expect a lightly doped emitter for recipe [D] compared to [C]. For recipe [E], ramp-up, drive-in and cool down steps were realized under O_2 ambient, meaning that Si interstitials are oxidized and P diffusion from PSG to Si wafer is blocked. The expectation is to get a lowly doped emitter. Finally, recipe [F] has the same process steps except for the deposition step. According to the recipe [E] results, $POCl_3/O_2$ gas ratio was changed to obtain an emitter profile suitable for the PERC with selective emitters.

STEP / RECIPE	Deposition	Ramp Up	Deposition	Drive-In	Cool Down-1	Cool Down-2	$POCl_3/O_2$ Ratio
[A]	@780°C for 10 minutes	to 830°C under N_2	@830°C for 12 minutes	830°C for 7 minutes under O_2 (Low O_2 Flow)	for 18 minutes		1000/1400 [sccm]
[B]	@780°C for 25 minutes						1000/1400 [sccm]
[C]	@780°C for 25 minutes	to 830°C under N_2		830°C for 15 minutes under N_2	for 15 minutes under N_2	for 15 minutes under N_2	1000/1400 [sccm]
[D]	@780°C for 25 minutes	to 830°C under N_2		830°C for 15 minutes under O_2	for 15 minutes under N_2	for 15 minutes under N_2	1000/1400 [sccm]
[E]	@780°C for 25 minutes	to 830°C under O_2		830°C for 15 minutes under O_2	for 15 minutes under O_2	for 15 minutes under N_2	1000/1400 [sccm]
[F]	@780°C for 25 minutes	to 830°C under O_2		830°C for 15 minutes under O_2	for 15 minutes under O_2	for 15 minutes under N_2	750/600 [sccm]

Figure 4.5. Process details of recipes

Active dopant profiles and average sheet resistances of the recipe [B], [C], [D] and [E] are shown in Figure 4.6. The result of the recipe [B] implies that a few numbers of P can diffuse into the Si wafer during the pre-deposition step at these conditions. As expected, the emitter formed by recipe [C] has the lowest sheet resistance value

and the highest number of dopants. For recipe [D], there is an increase in the sheet resistance due to the O_2 ambient during the drive-in step which implies that most of the P atoms have already been diffused into the Si wafer during the ramp-up and cool down steps. For recipe [E], as expected from the theory of $POCl_3$ diffusion, a huge amount of decrease in the dopants is observed compared to recipe [C] and [D]. However, some P atoms are still diffused into the Si wafer when comparing recipes [B] and [E].

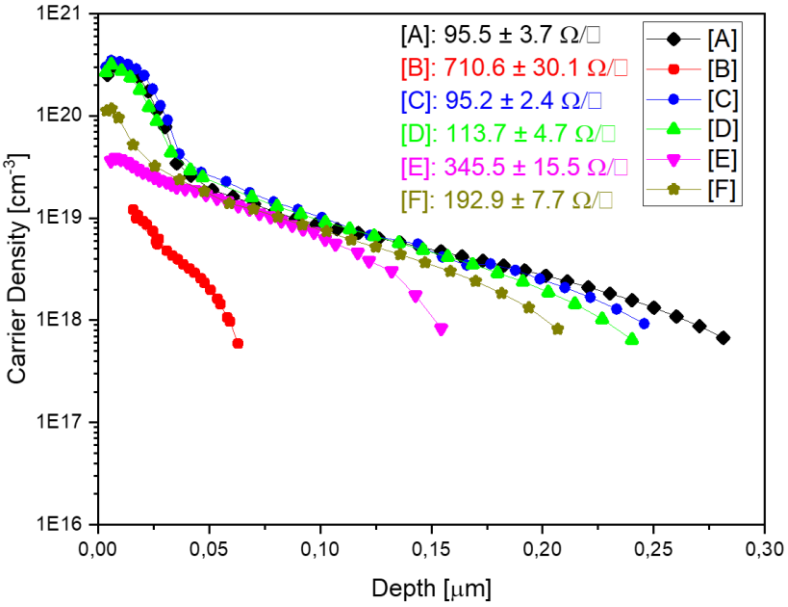

Figure 4.6. Active dopant profiles of recipes [A]-[F] measured by ECV

One possible reason is that the O_2 drive-in condition may not completely block the diffusion of P atoms. The other possible reason may be the inactive P atoms that have already been diffused into the Si wafer during the pre-deposition step. In addition, amount of P in the PSG layer is critical for selective emitter application, which is local laser doping process to obtain an emitter profile with high surface concentration and deep junction depth under the metallized area. To find the answers, three wafers were processed by using recipe [B] with $POCl_3/O_2$ gas ratio of 900/600 sccm. The first sample (B1) was cut in half and one part was annealed in a tube furnace after removing the PSG layer (B1-Annealed) while the other part was kept as control

group (B1-Control). The second sample (B2) was annealed in a tube furnace under N2 ambient at 875C for 40 minutes while keeping the PSG layer on the sample. Finally, the third sample (B3) was kept in the diffusion furnace after pre-deposition step and subjected to drive-in under N_2 at 875C for 40 minutes.

Active dopant profiles of the resulted profiles are given in Figure 4.7 while sheet resistances and doses are given in Table 4.1. The results show that increase in P atoms in the emitter during O_2 drive-in is that O_2 is unable to completely prevent the P diffusion from PSG to Si wafer. B1-Control and B1-Annealed profiles have similar sheet resistance values and doses calculated by numerical integration of the doping profile measured by ECV from surface to junction. This means that, there is no significant amount of inactive P in the emitter after the deposition. In addition, by annealing at high temperatures, it is proven that there is enough P in the PSG layer to form selective emitter. Amount of diffused P in the emitter is higher if the high temperature annealing process is applied in diffusion furnace (B3) instead of in clean tube furnace (B2). This may be due to the diffusion of P atoms from the environment (quartz tube and boat) to Si wafer in diffusion furnace.

Table 4.1. Sheet resistances and doses of the diffused regions before and after annealing with or without PSG layer is on the surface

Name	Sheet Resistance (Ω/□)	Dose (cm^{-2})
B1-Control	354	≈1.5E14
B1-Annealed	371	≈1.5E14
B2	85	≈7.7E14
B3	33	≈2.8E15

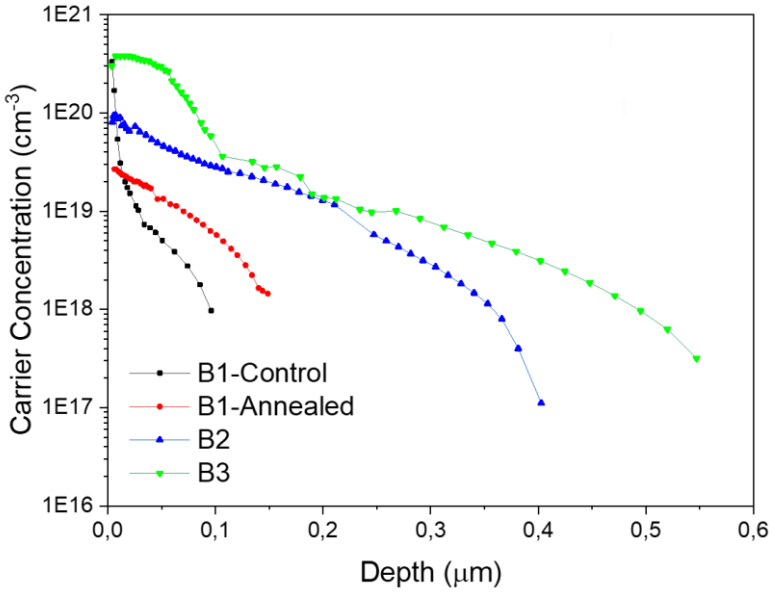

Figure 4.7. Active dopant profiles of the diffused regions before and after annealing with or without PSG layer is on the surface

To passivate the emitters, two different ARCs, SiN_x and SiO_xN_y, layers were used. It is also known that the thermally grown SiO_2 layer enhances chemical passivation. To see the effect of the SiO_2, both ARC layers are deposited alone and on the SiO_2 layer. After depositing the passivation layers, a firing study is held on and each group's best results are reported in Figure 4.8.

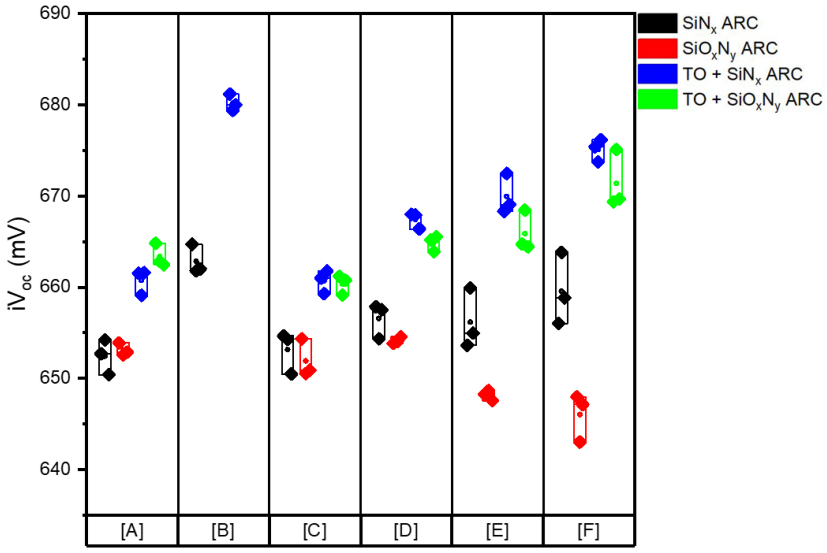

Figure 4.8. iV_{oc} results of 5 emitters with two different ARCs (SiN_x and SiO_xN_y) and with or without thermal oxide (TO)

QSSPC results of the symmetrically diffused and passivated with a stack of SiO_2/SiN_x samples are shown in Figure 4.9. The left y-axis (blue) represents $J_{0,e}$ values and the right y-axis (green) represents the estimated τ_{bulk} values. Another y-axis on the right represents the iV_{oc} values (red) on a scale from 620 to 690 mV. In the x-axis, values from F1 to F6 represent the different firing conditions in increasing order, F1 has the lowest and F6 has the highest peak firing temperature. Details of the firing profiles are shown in table.x.x. The results show that recipe [B] has the highest lifetime quality in every aspect (the lowest $J_{0,e}$ and the highest iV_{oc} and estimated τ_{bulk}) due to the very low doping concentration. $J_{0,e}$ values can be considered as same for all firing conditions. However, estimated τ_{bulk} values are reduced when the peak firing temperature increases. This may be caused by the Hydrogen (H) passivation since diffusion of H from SiN_x to Si is related to temperature. This situation is observed for all recipes. Recipes [A] and [C] have the highest doping concentrations due to all process steps except for pre-deposition, which are realized under ambient containing very low O_2 or totally in N_2. Due to

high doping concentration, Auger recombination increases. Thus, this leads to higher $J_{0,e}$ values than any other groups. Compared to recipe [C], recipe [D] has a smaller dead layer reflected on $J_{0,e}$ results. Also, iV_{oc} and estimated τ_{bulk} values are higher, indicating that recipe [D] should perform better on the cell level. Recipe [E] has lower $J_{0,e}$ values than recipe [D], but estimated τ_{bulk} values are also lower. This may be due to the reduction in the surface concentration, leading to a change in the H diffusion mechanism from passivation layers to Si wafer. Finally, by comparing recipe [D] and [E], recipe [F] has better lifetime quality in every aspect than these two recipes. The reason is that no dead layer formation is observed and sufficiently high surface concentration possibly helps to increase the estimated τ_{bulk}.

Table 4.2. Properties of the firing recipes

Firing Recipe Name	Peak Set Temperature (°C)	Belt Speed (cm/min)
F1	800	300
F2	800	380
F3	825	500
F4	850	500
F5	875	500
F6	900	500

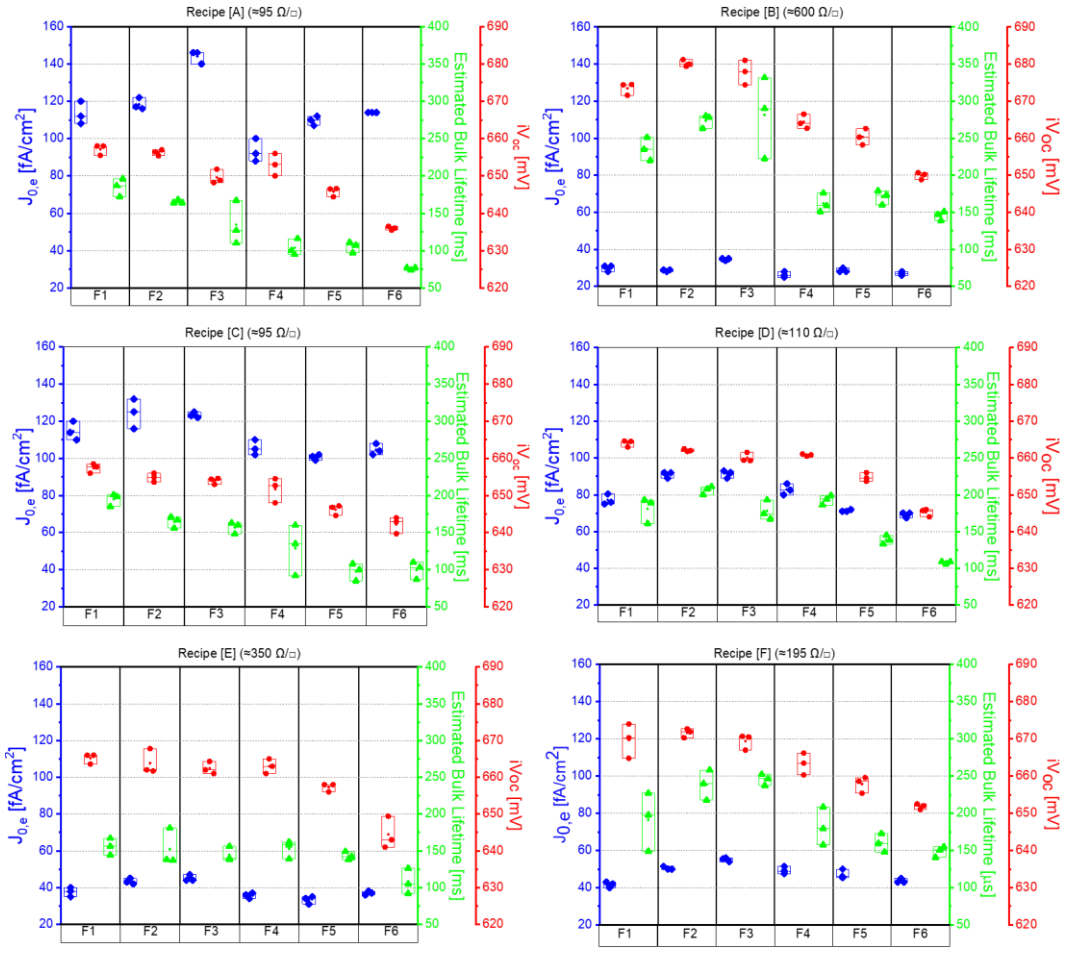

Figure 4.9. $J_{0,e}$, estimated bulk lifetime and implied V_{oc} (iV_{oc}) results of symmetrical emitter samples fabricated with 6 different emitter recipes, passivated with SiO_2/SiNx stack and subjected to different firing temperatures (F1-F6)

4.3 Performance Enhancement of PERC solar cell with SiO_xN_y Back Surface Passivation by LTA Process

4.3.1 Experimental Details

In this part of the study, the effect of LTA treatment on emitter passivation is studied. P-type, textured, industrial-size Cz-Si wafers with a resistivity of 1-3 Ω.cm and thickness of 180 µm were used as substrate. For the optimization of the LTA process,

symmetrical samples were fabricated by depositing a SiN_x layer on both sides of the wafers after the phosphorus diffusion with a resulting 90 Ω/□ emitter sheet resistance and 0.3 µm junction depth by using $POCl_3$ as the dopant source. Then, five different temperatures and two different durations were applied for LTA processes in a tube furnace under N_2 flow. Following the LTA, a fast-firing step was applied using an industrial conveyor belt furnace with a peak set temperature of 910°C. Quasi-steady-state photo conductance (QSSPC) method was used to characterize the symmetrical samples. After optimizing the LTA condition, PERC cells are fabricated. For the cell fabrication, textured wafers underwent through a phosphorus diffusion followed by the single side etching process for rear side emitter removal. While silicon oxynitride (SiO_xN_y) layer capped with SiN_x was used for passivation of the rear surface, SiN_x layer was used for the front surface. To see the effects of the optimized LTA process on cell performance, wafers were divided into two groups. One group of wafers was exposed to LTA while the other group was used as the control group. The rear side of the samples was ablated by a picosecond pulsed laser prior to metallization. Finally, metallization and firing processes were performed for contact formation. For the cell characterization, current-voltage (I-V) measurements were conducted with a class AAA solar simulator.

4.3.2 Results of the Symmetrical Samples

To reach the optimum condition for LTA, symmetrically phosphorus diffused and SiN_x passivated samples were processed in two different batches. For the first batch, as illustrated in Figure 4.10, two different annealing temperatures (600°C and 700°C) were applied for two different time periods (17 and 60 minutes). By comparing the iV_{oc} values "After diffusion" (black boxes) and "After SiN_x deposition" (blue boxes), it was observed that the samples were almost identical as expected. In the control group, samples were directly fast fired after SiN_x deposition (no LTA). The results show that if LTA process is conducted at 600°C, no significant change is observed in the after fast firing. On the other hand, LTA process at 700°C significantly

improves iV_{oc} values of the fired samples (named "After Firing") by approximately 10 mV regardless of duration. Hydrogen might be playing a role for the improvement of iV_{oc} since diffusion of H from SiN_x to Si depends on the temperature [15]. Moreover, the behavior between "After LTA" and "After Fast Firing" (red boxes) results should be taken into consideration. For the firing stability of the symmetrical samples, it is necessary to apply LTA process at a higher temperature and for a longer time. In the case of LTA at 600°C, iV_{oc} values decrease with a process time of 60 minutes. However, for 700°C and 60 minutes duration, iV_{oc} values or the passivation quality improves.

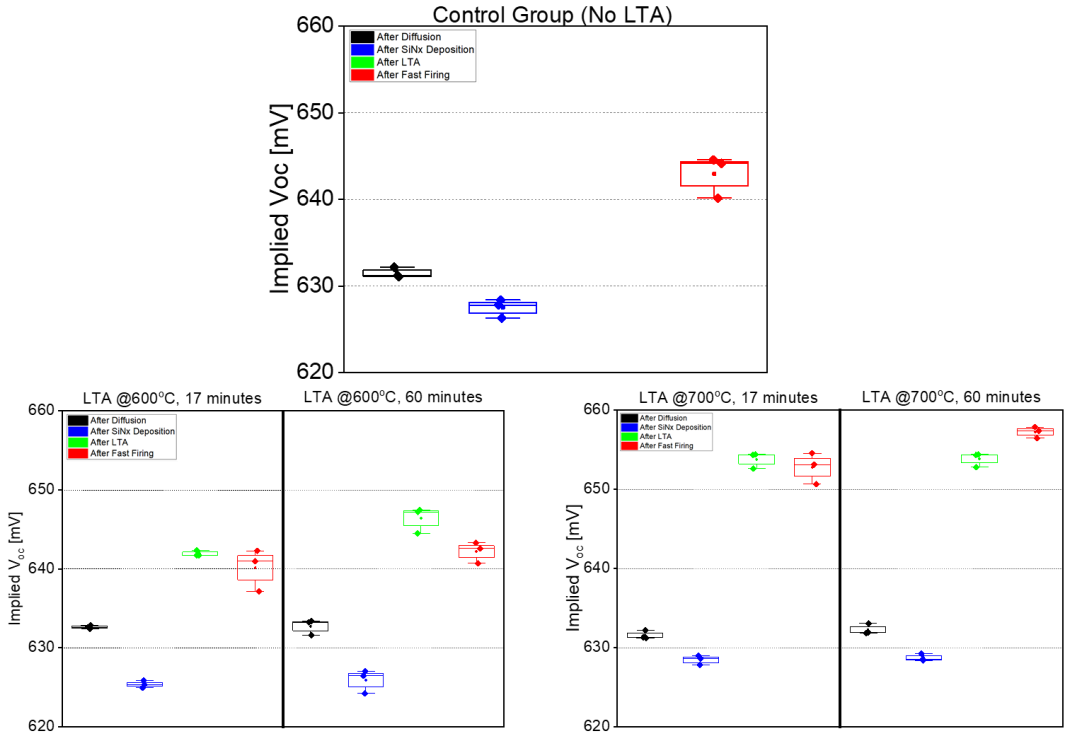

Figure 4.10. iV_{oc} results of the first batch of symmetrical emitter samples with no LTA treatment (control group), samples with LTA at 600°C for 17 and 60 minutes and samples with LTA at 700°C for 17 and 60 minutes

Comparing with the control group, LTA condition at 700°C for 60 minutes shows more than 10 mV improvement for the finished samples. According to the results of

the first batch, increasing LTA temperature enhances the iV_{oc} of the samples. Therefore, to investigate the higher temperatures above 700°C, we fabricated a second batch of symmetrical samples. In the second batch, three different LTA temperatures are applied to the group of samples as 700°C, which was the best LTA condition in the first batch and used as a reference, 725°C and 750°C for 17 minutes and 60 minutes. We also included reference samples without LTA.

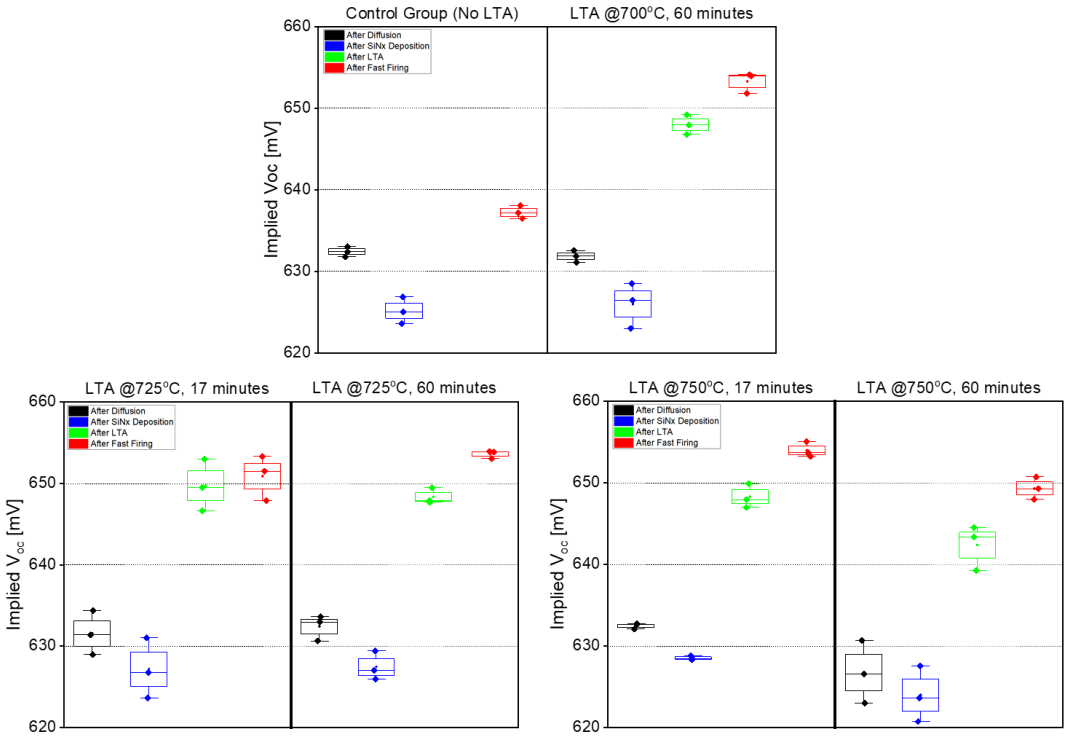

Figure 4.11. iV_{oc} results of the second batch of symmetrical emitter samples with no LTA treatment (control group) and LTA at 700°C for 60 minutes as a reference, samples with LTA at 725°C for 17 and 60 minutes and samples with LTA at 750°C for 17 and 60 minutes

Figure 4.11 shows the results of the second batch of samples. Regardless of the process time and temperature, more than 10 mV of iV_{oc} gain is observed and the same passivation quality is obtained for all LTA conditions. At 750°C, for 60 minutes of process time, the results are lower than the other LTA conditions. This

may be due to lower quality emitter, which can be deduced from the "After Diffusion" measurements results. Also, 17 minutes of process time for LTA at higher temperatures (725°C and 750°C) can be enough to reach almost the maximum iVoc values.

4.3.3 Results of the PERC Cells

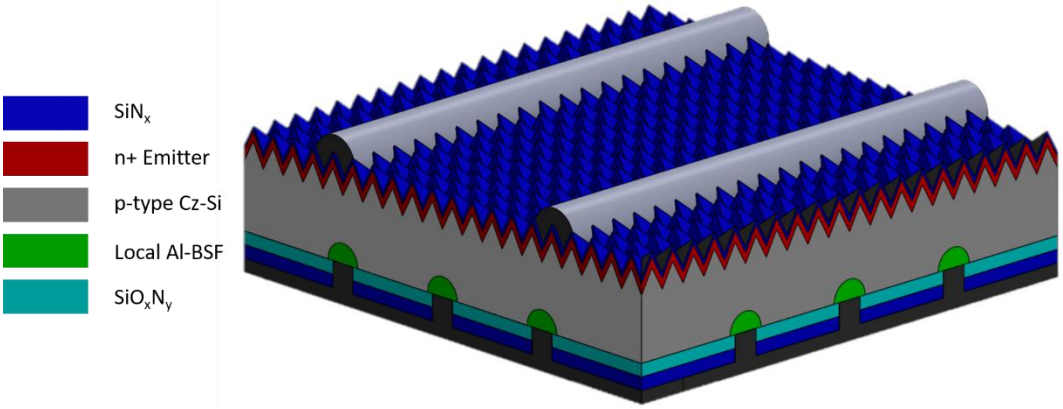

Figure 4.12. The schematic of the PERC solar cell

Process condition of LTA was chosen based on the results of symmetrical samples. Since 700°C for 60 minutes results in maximum iVoc values in both batches, this condition is applied for the fabrication of PERC solar cells. The study with the symmetrical emitter samples demonstrated that LTA has a major impact on the passivation of the emitter. For the next step, a new set of samples were fabricated to make PERC cells, the structure can be seen in Figure 4.12. Samples are divided into two groups to observe the effect of LTA. The first group of samples were fabricated without LTA process as a reference set while the second group of samples was exposed the LTA at 700°C for 60 minutes. For the rear surface passivation, SiO_xN_y was grown on the surface by using PECVD due to its thermal stability so that no degradation will occur during long LTA processes [35]. Figure 4.13 shows the results of the solar cells in terms of V_{oc}, J_{sc}, FF and efficiency. V_{oc} of the PERC cells with LTA treatment shows an approximately 10 mV increase, which is consistent with iV_{oc} results of symmetrically passivated emitter samples. Along with an increase in

V_{oc}, we obtained 0.4 mA improvement in average J_{sc} thanks to LTA process. Moreover, LTA does not affect the FF values of the device.

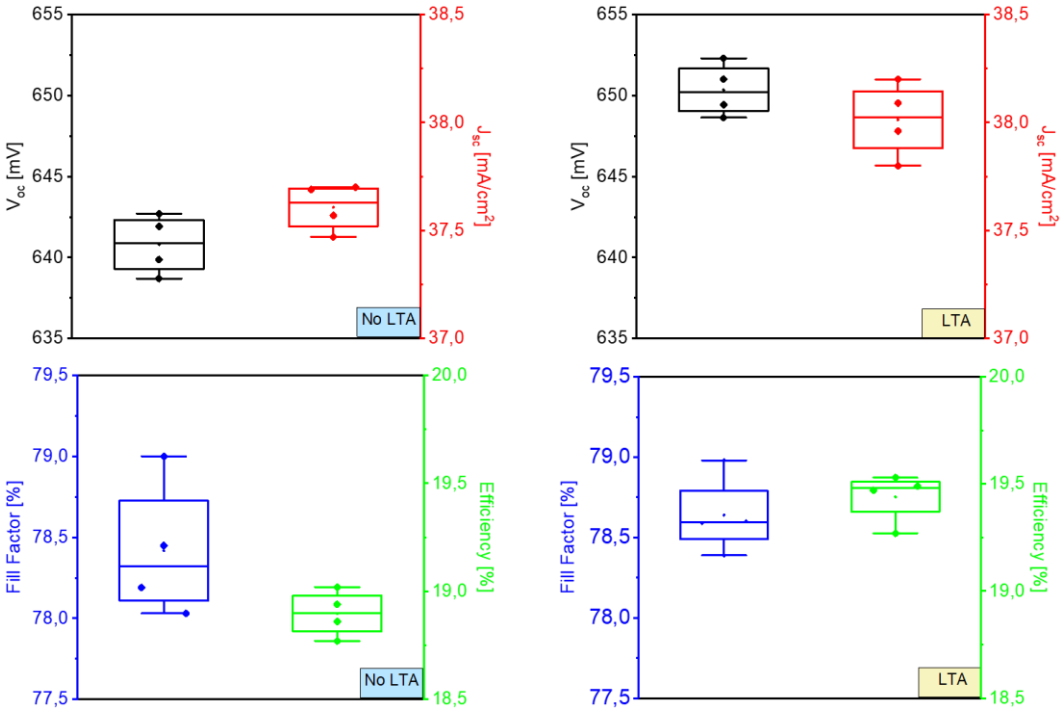

Figure 4.13. PERC cell results from I-V curve showing the effect of LTA on V_{oc}, J_{sc}, FF and efficiency on PERC cells fabricated without LTA (left) and PERC cells fabricated with LTA at 700°C for 60 minutes (right)

4.4 Emitters with Low Surface Concentration and Deep Junction

For diffused regions, Auger recombination is the dominant loss mechanism. Auger recombination limits the lifetime and ultimately the efficiency of the solar cell [23]. Carrier concentrations above 1E20 cm^{-3} for P-doped regions are called as dead layers due to the high level of Auger recombination. By reducing the surface concentration of the emitter, one can simply reduce the total recombination in the layer. In this part of the experiment, two different emitters having similar sheet resistance values but different surface concentrations are formed and the performance of these regions is characterized by symmetrical emitter samples and PERC solar cells.

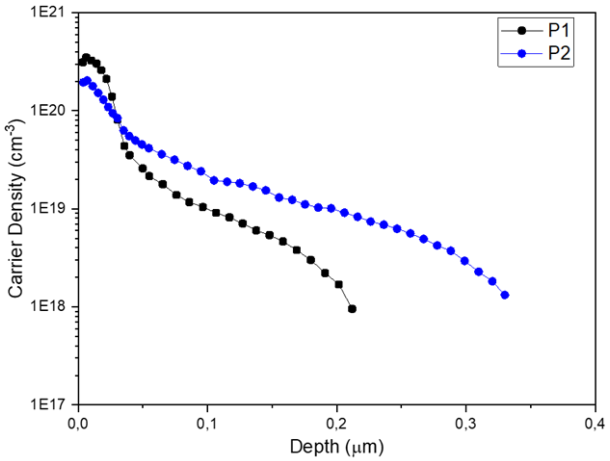

Figure 4.14 ECV measurement results of recipes P1 and P2

In Figure 4.14 active dopant profiles of emitter P1 and P2 are given. P1 has a high surface concentration (≈3E20 cm^{-3}) but a shallower junction, while P2 has a low surface concentration (≈2E20 cm^{-3}) but a deeper junction. Both emitters have the same sheet resistance value of 90 Ω/□. P1 is the recipe [C] in section 4.2. To form the emitter P2, the drive-in temperature of recipe [C] is increased from 830°C to 880°C while the drive-in duration is increased from 15 minutes to 40 minutes.

As much as the emitter profile, emitter passivation is critical to obtain reasonable lifetime values. In section 2.5, it is mentioned that a thin oxide layer grown on the samples by the LTO process is beneficial for the surface passivation of the n+ layer. Also, layer/s deposited by PECVD act as an H source to passivate both the surface and the bulk. In this study, two different ARCs deposited by PECVD are used. The first ARC, named as S1, is a SiNx:1/SiNx:2 stack layer, while the second ARC, named as S2, is a SiOxNy/SiNx:3 stack layer. Details of the layers are shown in Table 4.3. In addition, as it is mentioned in section 2.4, an LTA process can help to increase the surface and bulk passivation. It is already shown that in section 4.3, the LTA process increases the emitter passivation and consequently the cell efficiency.

Table 4.3. Properties of PECVD deposited layers

Name	Refractive Index	Thickness (nm)
SiNx:1	2.18	21
SiNx:2	1.99	55
SiNx:3	2.04	25
SiOxNy	1.73	64

In Figure 4.15, iV_{oc} results of the symmetrical emitter samples are shown. P1 and P2 represent the two emitter profiles, while with oxide and without oxide indicate whether the LTO process is applied or not, respectively. According to the results, as in section 4.2, a thin oxide layer enhances the emitter passivation. Moreover, depending on the ARC stack layers, LTA treatment can enhance or degrade the passivation quality of the emitter. If the LTA process is not applied to the samples, similar results are obtained for both S1 and S2 ARCs. However, S1 stack enhances the iVoc values for both emitters by increasing the LTA process temperature. On the other hand, for the S2 stack, increasing the temperature of LTA diminishes the iV_{oc} values. This can possibly be explained by the amount of H in the stack layers. iV_{oc} itself is not enough to give an idea about the H passivation. Therefore, $J_{0,e}$ and estimated bulk lifetime values are calculated and given in Table 4.4 and Table 4.5.

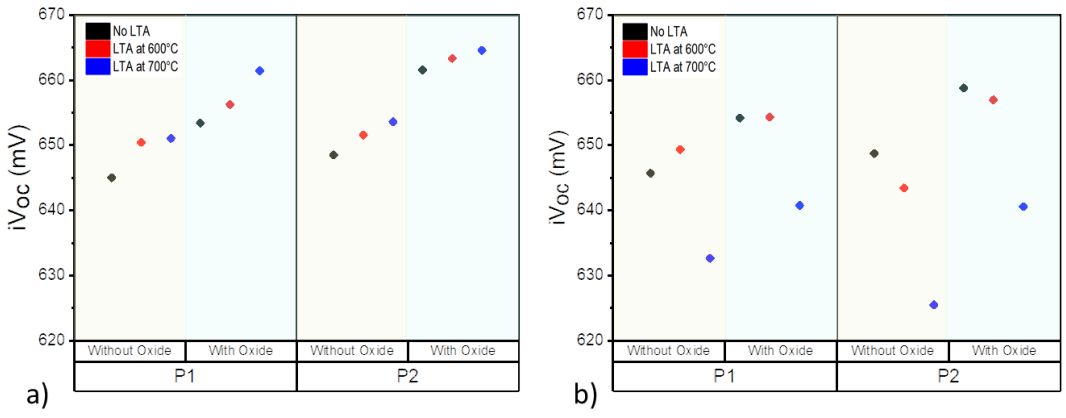

Figure 4.15. iV_{oc} results of symmetrical emitter samples passivated with ARC a) S1 (SiN_x stack) b) S2 (SiO_xN_y stack)

In Table 4.4, $J_{0,e}$ and τ_{bulk} results of emitter P1 are given. Comparing P1-A1 vs. P1-A4 and P1-B1 vs. P1-B4, without an LTA process, similar results are observed for both the SiNx and the SiOxNy ARC samples. However, if the samples have SiNx ARC, increasing the LTA treatment temperature results in an enhancement in the passivation quality. This may be related to sufficient H content in the H-rich SiNx:1 layer and during the annealing, these H atoms are released and passivate the surface and the bulk. On the other hand, if the samples have SiOxNy ARC, LTA at 600°C increases the bulk passivation while at 700°C, the process has detrimental effects on all lifetime values. This could be explained with no H-rich layer in the SiOxNy ARC stack and enhanced H diffusion at 700°C.

Table 4.4. $J_{0,e}$ and τ_{bulk} results of emitter P1

Sample Name	Thermal Oxide	ARC	LTA	$J_{0,e}$ (fA/cm^2)	τ_{bulk} (μs)
P1-A1	-	SiN_x	-	132	88
P1-A2	-	SiN_x	600°C	120	115
P1-A3	-	SiN_x	700°C	132	169
P1-A4	-	SiO_xN_y	-	142	89
P1-A5	-	SiO_xN_y	600°C	140	134
P1-A6	-	SiO_xN_y	700°C	257	55
P1-B1	Thin Ox	SiN_x	-	100	130
P1-B2	Thin Ox	SiN_x	600°C	90	148
P1-B3	Thin Ox	SiN_x	700°C	83	229
P1-B4	Thin Ox	SiO_xN_y	-	103	134
P1-B5	Thin Ox	SiO_xN_y	600°C	105	163
P1-B6	Thin Ox	SiO_xN_y	700°C	168	78

In Table 4.5, $J_{0,e}$ and τ_{bulk} results of emitter P2 are tabulated. The same trends for both the SiN_x and the SiO_xN_y ARC samples are observed, but the changes in the lifetime values in SiNx ARC samples are not as significant as the emitter P1. This may be explained by the low surface concentration of the emitter P2 and its relation with the H diffusion.

Table 4.5. $J_{0,e}$ and τ_{bulk} results of emitter P2

Sample Name	Thermal Oxide	ARC	LTA	$J_{0,e}$ (fA/cm^2)	τ_{bulk} (μs)
P2-A1	-	SiN_x	-	122	116
P2-A2	-	SiN_x	@600°C	110	127
P2-A3	-	SiN_x	@700°C	108	138
P2-A4	-	SiO_xN_y	-	116	97
P2-A5	-	SiO_xN_y	@600°C	150	83
P2-A6	-	SiO_xN_y	@700°C	313	44
P2-B1	Thin Ox	SiN_x	-	60	163
P2-B2	Thin Ox	SiN_x	@600°C	62	206
P2-B3	Thin Ox	SiN_x	@700°C	65	214
P2-B4	Thin Ox	SiO_xN_y	-	76	153
P2-B5	Thin Ox	SiO_xN_y	@600°C	84	140
P2-B6	Thin Ox	SiO_xN_y	@700°C	175	85

According to the results obtained from the symmetrical emitter samples, for both emitter P1 and P2, the SiN_x stack is chosen as ARC and the temperature of LTA is determined as 700°C. The process flow of the fabricated PERC cells is shown in Figure 4.16. After the ARC deposition, the samples are divided into two groups. The first group of samples follows the standard PERC cell fabrication route, while the second group is subjected to LTA treatment at 700°C and then follows the same route as the first group.

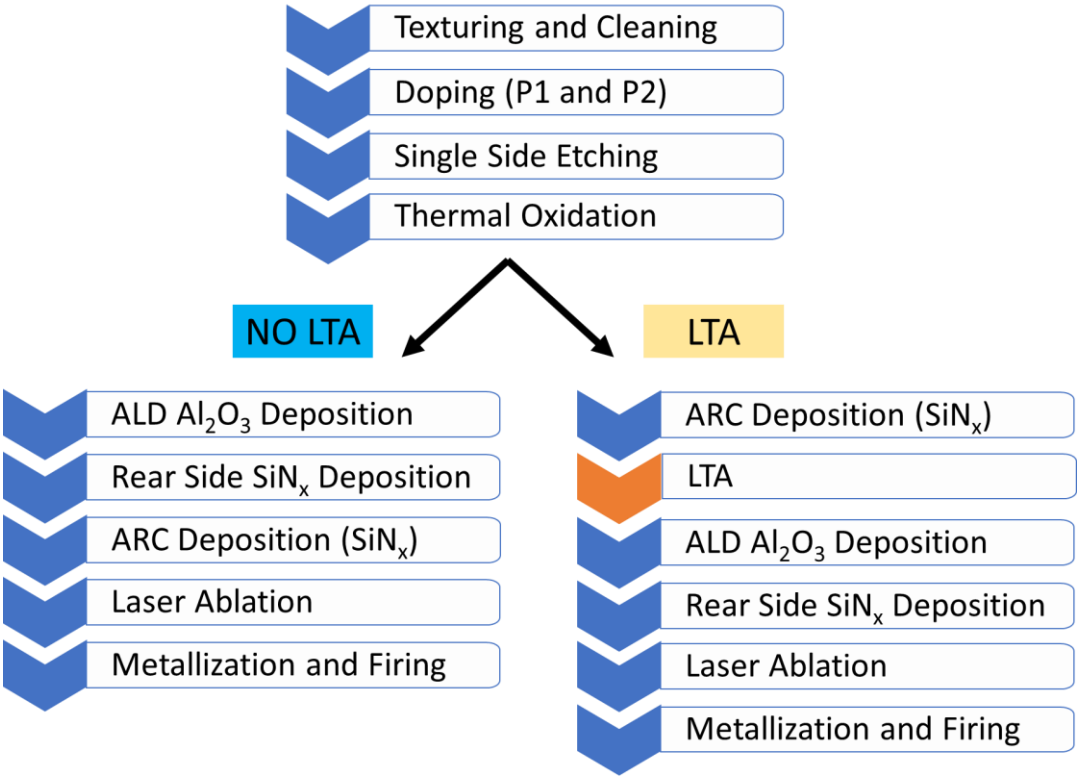

Figure 4.16. Fabricated PERC cells process flows with and without LTA treatment

Figure 4.17 shows the results of the PERC solar cells, which have emitter P1, with and without LTA treatment. The samples subjected to LTA treatment have more than 0.5%abs FF losses compared with the no LTA group and show larger dispersion in V_{oc} and J_{sc} values. Symmetrical emitter samples indicated that emitter passivation enhanced with the LTA treatment, but unlike in section 4.3, this effect is not observed in the PERC samples. One possible explanation is the passivation strategy at the rear side passivation. To avoid the harmful effect of LTA on Al_2O_3/SiN_x stack passivation at the rear side, LTA treatment is applied first, as it is shown in Figure 4.16. A more convenient way is to use SiO_xN_y instead of a thin Al_2O_3 layer. Another way is to optimize Al_2O_3/SiN_x or Al_2O_3/SiO_xN_y stacks that provide enough H and fixed charge passivation when the samples are subjected to LTA treatment. By comparing the two groups of samples (No LTA and LTA), similar Voc and Jsc values are measured despite the difference in rear side passivation strategy

depending on the samples. This is due to the losses in the front contact areas compensating the gain in emitter passivation.

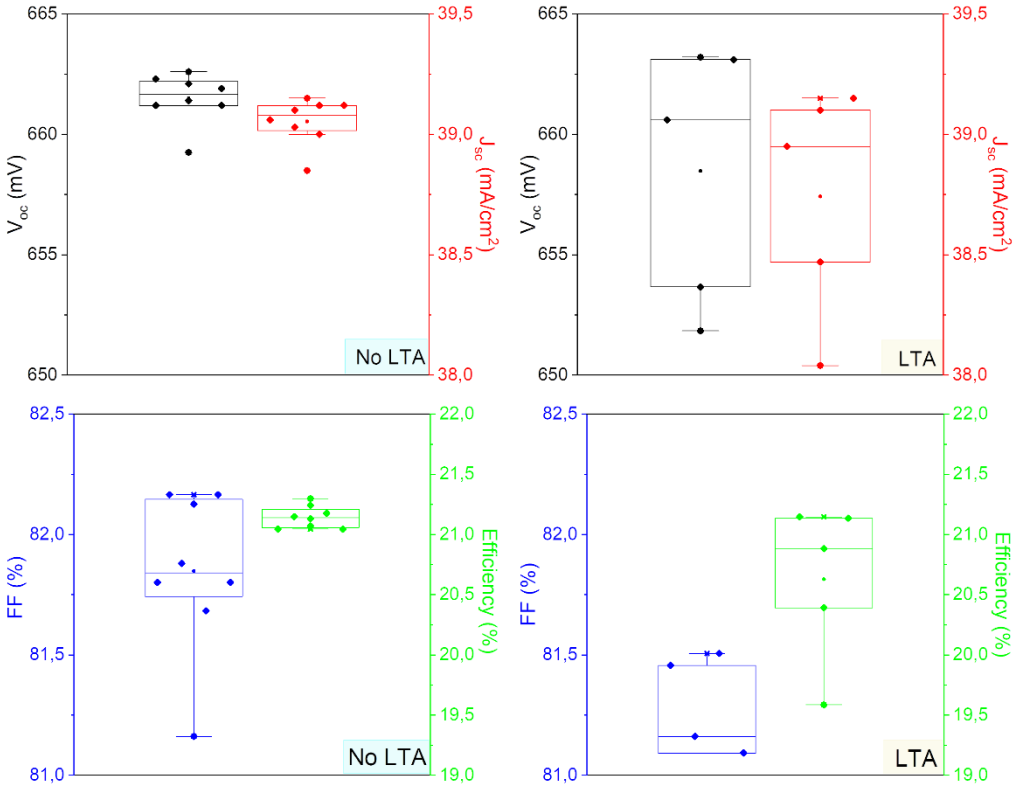

Figure 4.17. IV results of the PERC cells fabricated with emitter P1

To investigate the difference between the FF values of No LTA and LTA groups, solar cells are cut into TLM stripes as in Figure 3.22. The measured contact resistivity between emitter P1 and Ag contacts is shown in Figure 4.18. FF values of the cells used for the TLM measurements are 81.88% and 81.51% for no LTA and LTA samples, respectively. It is clearly seen that the contact resistivity is affected by the LTA process. The possible reason is H diffusion and its effect on contact between the emitter and the metal.

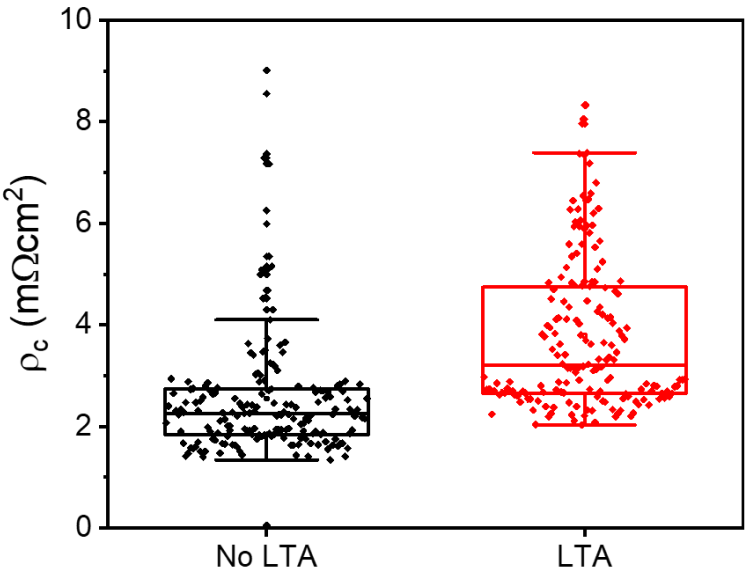

Figure 4.18. Contact resistivity between Ag paste and emitter P1

The expectation for PERC cells fabricated with emitter P2 is to obtain higher PCE than those fabricated with emitter P1. However, the IV results shown in Figure 4.19 show the opposite. Low FF values indicate that firing conditions are not suitable for emitter P2. On the symmetrical emitter samples, firing conditions do not have harmful effects on lifetime values as it is shown in Figure 4.15 and Table 4.5. On the other hand, changes in the surface concentration of the active dopant profiles decrease the contact quality under the same firing conditions. Low contact quality can cause an increase in resistance and in the recombination under metal contacts. Therefore, a firing study should be conducted to improve the contact between the emitter and metal.

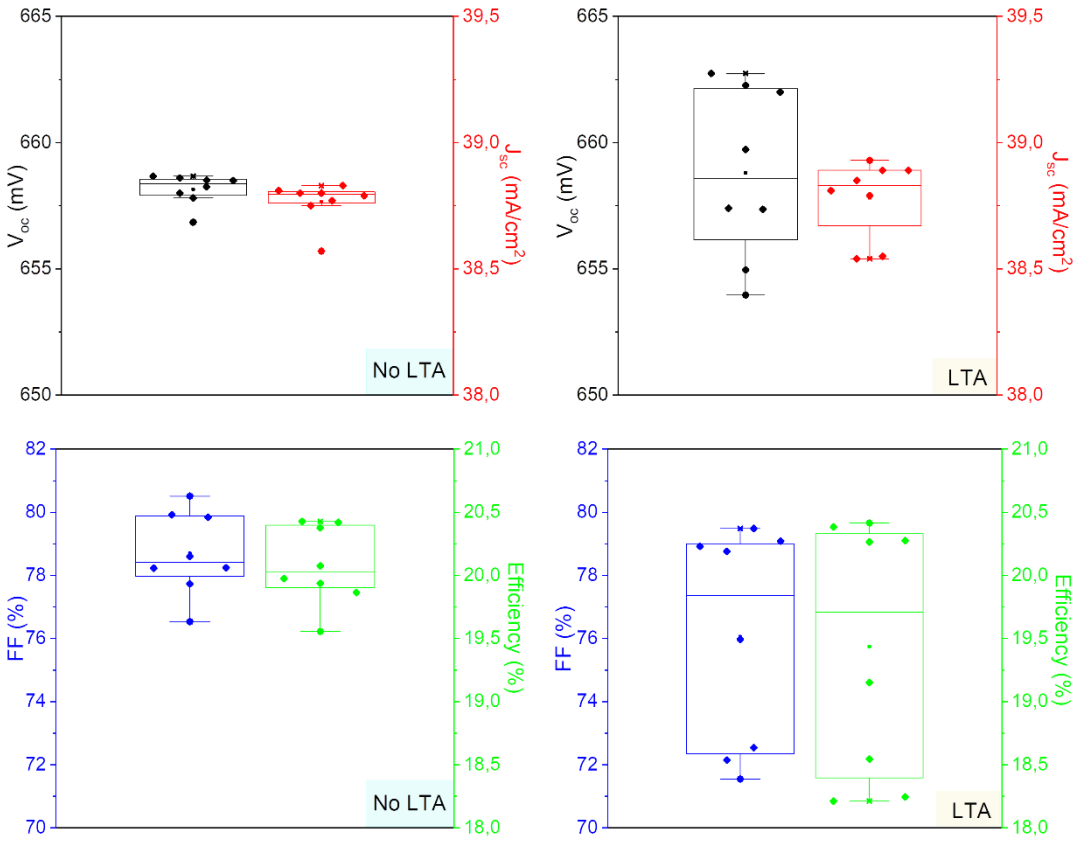

Figure 4.19. IV results of the PERC cells fabricated with emitter P2

Contact resistivities between the emitter P2 and Ag contacts are shown in Figure 4.20. The FF of the cells measured are 78.6% and 79.49 for no LTA and LTA groups, respectively. The difference between the contact resistivity values of emitter P1 and P2 is huge. This difference can lead to a decrease in FF values for P2 and so the PCEs.

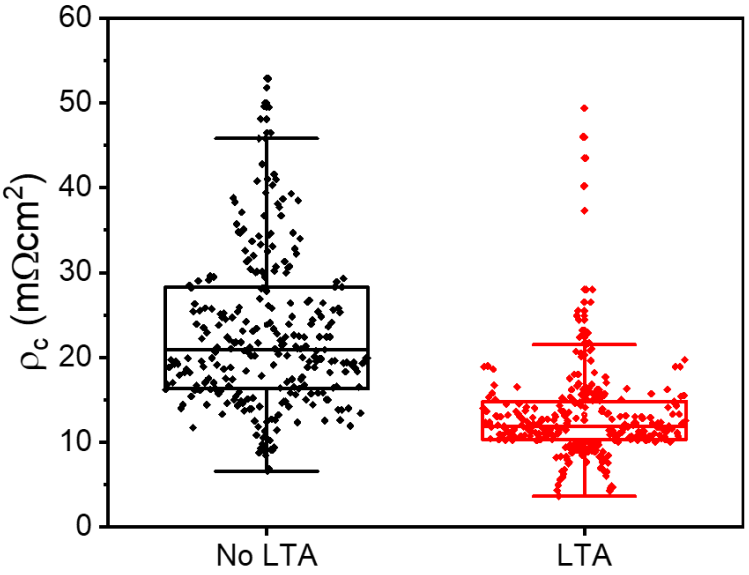

Figure 4.20. Contact resistivity between Ag paste and emitter P2

CHAPTER 5

CONCLUSIONS

In this thesis, the optimization of the n+ emitter profile and its passivation are studied. The active dopant profile of the formed emitters was measured with ECV, while the sheet resistances were measured with 4PP. Then, after the passivation, lifetime values were extracted from symmetrical emitter samples using the Sinton WCT120TS device. To form P-doped emitter regions, $POCl_3$ was used as a liquid source for diffusion processes. To passivate the surface of emitters, dry oxide grown in a tube furnace at a relatively low temperature (600°C) along with SiN_x and SiO_xN_y layers deposited by PECVD were used.

First, the effect of the number of wafers used for the diffusion process is investigated. The same diffusion recipe has experimented with 200 wafers and 68 wafers. The sheet resistance of the emitter increases as the number of wafers increases. This means fewer dopants diffuse into Si wafers if the distance between the Si wafers decreases. Moreover, using more wafers causes non-uniformity on the surface. As a result, the next experiments were conducted with a boat configuration with 68 wafers.

$POCl_3$ diffusion processes are carried out with N_2, O_2 and N_2-carried $POCl_3$ flows. It is known that $POCl_3/O_2$ gas ratio during the pre-deposition step determines the amount of P diffuses into Si. Along with pre-deposition, drive-in conditions also have impacts on the emitter profile. If the drive-in step is under the O_2 ambient, O_2 oxidizes the Si interstitials and blocks the P diffusion into Si. On the other hand, during the N_2 drive-in, Si interstitials are free to move to PSG and form free P atoms which diffuse to the Si wafer. Active dopant profiles were shown that the surface concentration of the emitter decreases drastically under O_2 ambient. To optimize the

surface concentration, $POCl_3/O_2$ gas ratio was increased and an emitter suitable for selective emitter applications was obtained.

To further improve the passivation quality of the emitter, an LTA process was implemented after the SiNx deposition was optimized. At 700°C for 1 hour is the optimized LTA condition to increase device performance on PERC solar cells with SiO_xN_y passivation layer at the rear side. LTA process after PECVD:SiN_x resulted in 10 mV gain in V_{oc} along with a 0.25 mA increase in Jsc. The result of the symmetrical samples implies that this increase in cell performance is related to the enhanced passivation of the emitter.

The dead layer in the emitter region leads to increase recombination due to high dopant concentration. Reducing the surface concentration of the emitter without changing the sheet resistance is an option for reducing $J_{0,e}$ without using selective emitter. Symmetrical emitter samples showed that equal or more than 5 mV gain in iVoc values are observed for the emitter with low surface concentration. Moreover, 40 fA/cm^2 less $J_{0,e}$ and 60 μs higher estimated τ_{bulk} were measured without an LTA process. Since the same firing conditions are used for both high and low surface concentration emitters, emitter-Ag contact became very resistive for the low surface concentration emitter. A firing study should be held on to improve the contact quality.

In conclusion, enhancements in the emitter profile, passivation and LTA conditions are promising for fabricating high-efficiency PERC solar cells. A metallization-firing study can be helpful in increasing efficiency due to improvements in the contact regions. In the future, cells with selective emitter will allow using emitter with lower surface concentration and fewer dopants.

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